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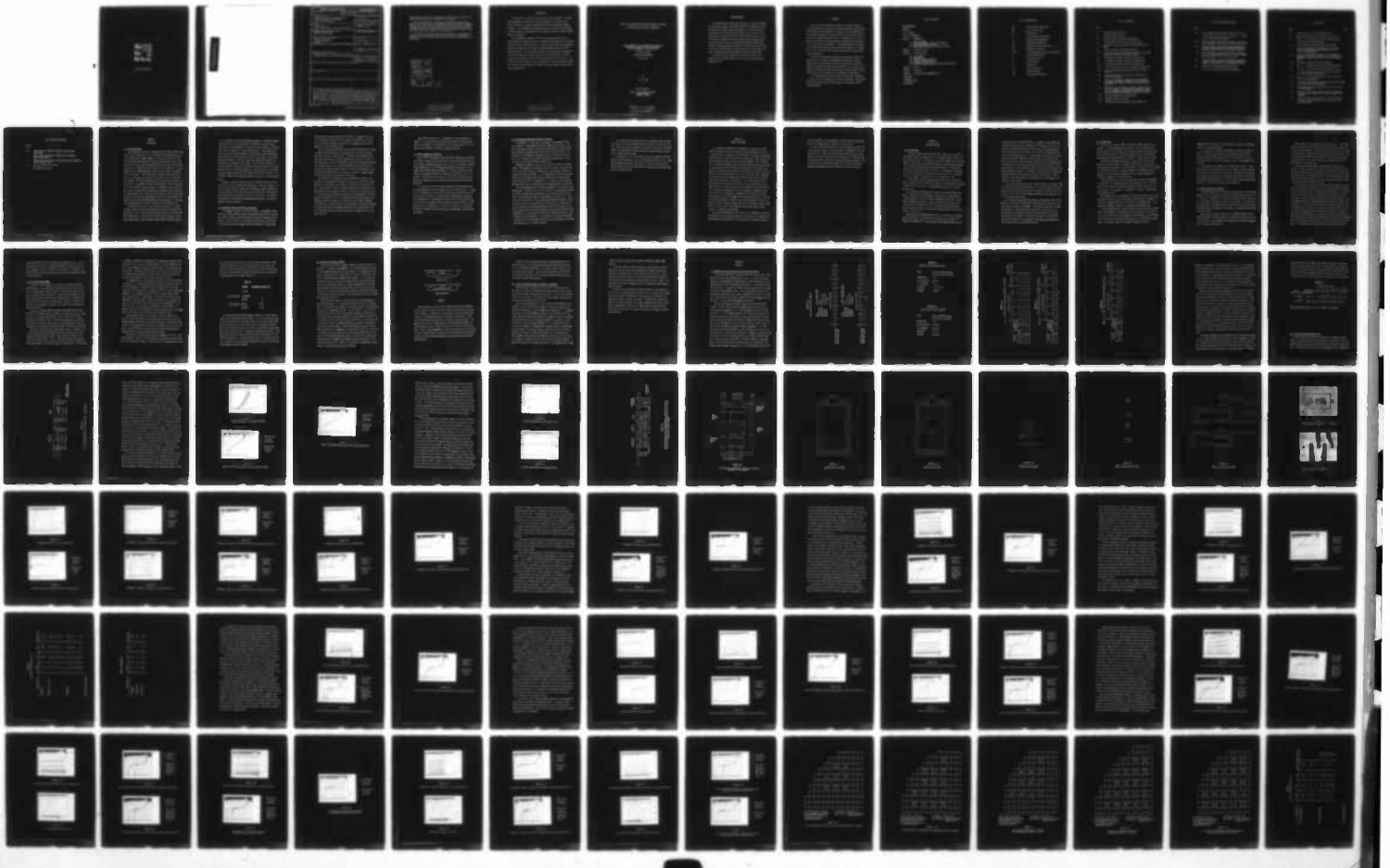

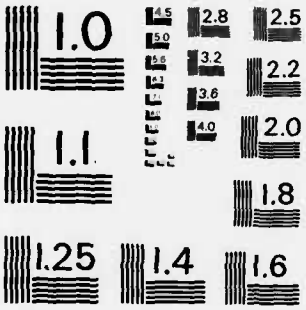

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High Concentration phosphorus diffusions into single crystalline silicon damages the silicon material producing anomalous diffusion effects and degrading device performance. Dislocations and a supersaturation of point defects are created to reduce the lattice strain caused by the presence of the undersized phosphorus atoms. A consequence of the lattice damage is the emitter push effect observed in double diffused structures (i.e., bipolar junction transistors). Simultaneous phosphorus and arsenic diffusions from CVD dual dopant

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SiO_2 sources are reported by M. Watanabe et. al.[3] to be dislocation free and eliminate emitter push in double diffused structures.

This study investigated the effects of simultaneous phosphorus and arsenic drive-in diffusions from predeposition diffusions using dual dopant SiO_2 spin-on sources on emitter push and dislocation generation. Although no reduction in emitter push was observed in this study, a minimization in dislocation density was exhibited in the dual dopant diffused layer surfaces near the optimum ratios reported by M. Watanabe et. al.

It is recognized that both the present study and the M. Watanabe et.al., study are early investigations into this new technology. Both studies indicate that this new process shows promise to improve semiconductor device performance.

INTRODUCTION

This document is a copy of the M.S. thesis of Mr. Paul Saka. It deals with development of a method for very heavy doping of silicon with low defect generation. Doping-induced damage can lead to undesirable leakage currents. Since homojunction subbanding structure can require heavy doping, (it affects degree of confinement and quantization), control of dopant induced damage is desirable.

The simultaneous diffusion of As and P from spin-on SiO_2 sources is investigated in an attempt to evolve a convenient technology for high impurity concentration low defect generation, in bipolar devices (including subbanding devices) and improvement in junction isolation behavior under very high doping conditions. The diagnostics use bipolar transistor emitter push/pull to characterize impurity induced strain and strain compensation. Results indicate an improvement in lattice strain at particular ratios of As/P. The investigation also suggests that the technology has complex phenomena involved. Our results indicate that R&D are indicated in before commercial application would be appropriate.

EFFECTS OF SIMULTANEOUS PHOSPHORUS AND ARSENIC DIFFUSIONS ON EMITTER PUSH AND DISLOCATION GENERATION

A THESIS SUBMITTED TO THE GRADUATE DIVISION OF THE
UNIVERSITY OF HAWAII IN PARTIAL FULFILLMENT
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IN ELECTRICAL ENGINEERING

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By

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ABSTRACT

High concentration phosphorus diffusions into single crystalline silicon damages the silicon material producing anomalous diffusion effects and degrading device performance. Dislocations and a supersaturation of point defects are created to reduce the lattice strain caused by the presence of the undersized phosphorus atoms. A consequence of the lattice damage is the emitter push effect observed in double diffused structures (i.e., bipolar junction transistors). Simultaneous phophorus and arsenic diffusions from CVD dual dopant SiO_2 sources are reported by M. Watanabe et. al. [3] to be dislocation free and eliminate emitter push in double diffused structures.

This study investigated the effects of simultaneous phosphorus and arsenic drive-in diffusions from predeposition diffusions using dual dopant SiO_2 spin-on sources on emitter push and dislocation generation. Although no reduction in emitter push was observed in this study, a minimization in dislocation density was exhibited in the dual dopant diffused layer surfaces near the optimum ratios reported by M. Watanabe et. al.

It is recognized that both the present study and the M. Watanabe et. al. study are early investigations into this new technology. Both studies indicate that this new process shows promise to improve semiconductor device performance.

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LIST OF ABBREVIATIONS

ASF	Arsenosilicafilm (Emulsitone)
ASG	arseno-silicate glass
BN	boron nitride
C_d	critical dopant ccncentration
C_s	dopant surface concentration
CVD	chemical vapor deposition
PSF	Phosphorosilicafilm (Emulsitone)
PSG	phosphoro-silicate glass
P-120	Accuspin phosphorus source (Allied Chemical)
SF	Silicafilm (Emulsitone)
$\bar{x}$	standard deviation
x_j	junction depth
ρ	resistivity
$\bar{\rho}$	average resistivity
ρ'_s	sheet resistance
$\bar{\rho}'_s$	average sheet resistance

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CHAPTER 1

INTRODUCTION

1.1 Problem Statement

High temperature diffusion is commonly used to introduce dopant atoms into silicon. These diffusions are performed at high temperatures using high concentrations of dopant atoms to try to minimize diffusion times. The high concentrations of dopant atoms also enhance certain device characteristics. However, the high temperature and high dopant concentration diffusions often damage the single crystalline silicon material. The high temperatures can produce thermally induced lattice stresses that damage the silicon material. High concentrations of dopant atoms dissimilar in size to silicon atoms also create lattice stresses that can cause additional damage. The lattice damage, primarily dislocations, vacancies, and interstitials, are created to reduce lattice stresses. Careful processing can minimize thermally induced stresses. The amount of stress created by the presence of dopant atoms is dependent on the dopant atom concentration and the difference in size between the dopant atoms and host crystal atoms. Frequently, the diffusion induced damage occurs in the active region(s) of the device fabricated thereby degrading device performance. The reduction of such damage generally results in improved device characteristics.

The diffusion profile of single diffused structures (i.e., diodes, resistors, ohmic contacts) exhibit anomalous profiles at high dopant concentrations. Pile up and precipitation of dopant atoms is also observed at high concentrations. The additional stresses caused by the pile up and precipitated dopant atoms can create defects. Double diffused structures

(i.e., transistors) show further anomalous phenomena. Conventional double diffused transistor structures exhibit a cooperative diffusion effect. This effect is the enhancement or retardation of the diffusion of a dopant species by the presence of a second dopant species. In npn transistors this effect causes the boron doped base region below a heavily doped phosphorus emitter to diffuse faster than the rest of the base. This emitter push effect produces a wider base region than expected and edges at the periphery of the pushed out base region. A similar type of cooperative diffusion effect is observed in pnp double diffused structures with a boron doped emitter and a phosphorus doped base. The emitter push is attributed to lattice damage caused by the high concentration emitter diffusion. This diffusion induced lattice damage enhances the diffusion of the base dopant atoms.

Anomalous diffusion effects occurring in the active regions of transistors can seriously degrade device performance. The lattice damage in the base and emitter regions increases base recombination current thereby reducing transistor current gain. The wider base region due to emitter push also reduces gain and increases transistor switching times. The edges at the periphery of diffused regions concentrate the electric field causing premature junction breakdown.

1.2 Conditions Affecting Dislocation Generation

It is commonly desirable to perform diffusions at high dopant concentrations to reduce diffusion times or enhance device performance. However, the resultant lattice stresses caused by the diffusion of dopant atoms dissimilar in size to silicon (i.e., phosphorus, boron) create dislocations [1] [2] which can seriously degrade device performance. At lower dopant

concentrations dislocation generation is minimal. The upper limit or C_d (critical dopant concentration) for dislocation free diffusion is sensitive to the type of dopant source used, initial condition of the silicon material, and diffusing conditions.

The C_d of $POCl_3$ and BN (boron nitride) sources are reportedly an order of magnitude less than those of PSG (phosphoro-silicate glass) and BSG (boro-silicate glass) sources [3] [4]. The dopant surface concentration from $POCl_3$ and BN sources frequently exceed the solid solubility limit of the dopant atoms in the silicon material at the diffusing conditions whereas silicate glass sources allow control over dopant surface concentrations. Precipitation of dopant atoms increases as the dopant concentration in the semiconductor approaches the solid solubility limit [5]. Stresses around these precipitates can also generate dislocations.

The presence of dislocations in the silicon material reduces C_d for dislocation free phosphorus diffusions. The C_d for dislocation free boron diffusions is reportedly not affected by the presence of dislocations [3] [4]. N-type doping of silicon increases the mobility of dislocation in the semiconductor while no change in mobility is observed in p-type doping [6]. It is postulated that additional dislocations can be generated by the movement of dislocations [7]. Thus the presence of dislocations reduces C_d for phosphorus diffusions whereas C_d for boron diffusions remains unchanged. The difference in dislocation mobility also resulted in dislocations created by n-type diffusions that penetrated deeper than the diffused layer while all dislocations created by p-type diffusions were located within the diffused layer [4].

The diffusing conditions (i.e., temperature, time) also affects C_d. However, it is reported that the critical total amount of diffused boron atoms for dislocation free BSG diffusions has a constant value of 1.6×10^{16} atoms per cm^2 regardless of diffusing conditions [3] [4].

1.3 Strain Compensation Diffusion

Strain compensation methods have been shown to reduce lattice stresses and produce dislocation free diffusions with dopant concentrations above C_d. The diffusion of dopant atoms smaller than silicon (i.e., phosphorus, boron) create compressional lattice stresses that generate dislocations. Strain compensation methods reduce the compressional lattice stresses by an additional or simultaneous diffusion of atoms larger than silicon (i.e., tin, gallium). The oversize atoms create dilational lattice stresses that compensate the compressional lattice stresses thereby preventing dislocation generation.

T.H. Yeh and M.L. Joshi [8] report dislocation free diffusions above C_d by simultaneously diffusing phosphorus and tin or boron and tin. K. Yagi et. al. [9] measured the lattice strain of phosphorus diffused layers from the rocking curve using a x-ray double crystal spectrometer. They report strain compensation in the phosphorus diffused layer by a pre-diffusion of tin as long as the phosphorus surface concentration was limited to 4×10^{20} atoms per cm^3. M. Watanabe et. al. [3] and K. Nishida et. al. [10] report dislocation free boron diffusions above C_d by simultaneously diffusing boron and gallium.

1.4 Simultaneous Phosphorus and Arsenic Diffusion

M. Watanabe et. al. [3] report dislocation free phosphorus diffusions above C_d by simultaneously diffusing phosphorus and arsenic. They also report the elimination of emitter push using a BSG diffused base and simultaneous PSG and ASG (arseno-silicate glass) diffused emitter. The optimum ratio of phosphorus to arsenic varies with diffusing conditions. For a four hour diffusion at 1000°C, the reported optimum ratio is $P:A_s$ = 3:1 and for a four hour diffusion at 1100°C, 4:1.

Phosphorus is smaller in size than silicon while arsenic is slightly larger. High concentration phosphorus diffusions create a supersaturation of vacancies that form vacancy clusters [11]. These vacancy clusters can extend into dislocation loops (i.e., are nucleating sites for dislocations). Arsenic diffusions deplete the vacancy concentration by forming vacancy-arsenic complexes [12]. M. Watanabe et. al. [3] report that simultaneous phosphorus and arsenic diffusions prevent the supersaturation of vacancies.

The proposed mechanism for dislocation prevention is not totally strain compensation. The lattice strain at the surface of a simultaneous phosphorus and arsenic diffused layer, measured using x-ray double crystal diffraction, is reportedly lower than in a phosphorus only diffused layer. However, the lattice strain in the diffused layer remained unchanged. Near the surface the pile up of arsenic atoms at off-lattice sites is observed at high concentration simultaneous phosphorus and arsenic diffusions. Dislocation formation at the surface is thought to be prevented by lattice strain compensation of the off-lattice arsenic atoms. Although the strain in the diffused layer was unchanged, it is postulated that dislocation formation is prevented in the simultaneous diffusions by the elimination of dislocation nucleating sites (i.e., vacancy clusters).

It is widely believed that emitter push is caused by excess vacancies as a result of the heavy phosphorus emitter diffusion [13] [14] [15] [16] [17]. The excess vacancies enhances the diffusion of the boron base dopant atoms. The simultaneous diffusions prevent the supersaturation of vacancies, eliminating emitter push.

M. Watanabe et. al. [3] also report that the simultaneous diffusions improve device performance. They cite reduced base-emitter junction recombination/generation current and reduced low frequency transistor noise. They also point out that the elimination of emitter push allows more precise control of the base width.

CHAPTER 2

PURPOSE AND SCOPE

This study was undertaken to investigate high concentration simultaneous phosphorus and arsenic diffusions. The simultaneous diffusions are reported by M. Watanabe et.al. [3] to produce high dopant concentration diffusions that are dislocation free and reduce emitter push in double diffused structures, thereby improving device performance. The M. Watanabe et.al. results were obtained from simultaneous phosphorus and arsenic deposition diffusions using CVD (chemical-vapor deposited) dual dopant SiO_2 sources. The present study monitored the effects of the simultaneous phosphorus and arsenic diffusions after a drive-in diffusion from a predeposition diffusion using dual dopant SiO_2 spin-on sources. Thus the present study differed from the M. Watanabe et.al. work in two aspects; type of dual dopant source used and the inclusion of a drive-in diffusion in the present study. The drive-in diffusion was included in the present study to try to determine the applicability of the simultaneous phosphorus and arsenic diffusions to conventional integrated circuit diffusion processes which usually involves both predeposition and drive-in diffusions. Arsenic spin-on dopant sources are commonly used in the semiconductor industry because the spin-on source provides a convenient and inexpensive dopant source that is relatively safer to use than the other arsenic dopant sources (arsenic is reportedly a carcinogen).

The present study focused on the effect of the simultaneous diffusions on emitter push and dislocation generation. The decision to concentrate on these aspects were determined in part by the ability to devise testing and

observation methods with the equipment and time available and considerations of scope appropriate for a master of science thesis.

Transistor gain measurements were taken to determine the gain sensitivity to monitor changes in the base width and recombination current in the base region. Scanning electron microscopic observation of cleaved transistor structures and lap and stain techniques were tested and the junction delineation capabilities of the two methods were examined. The dislocation etch pit delineation capabilities of several dislocation etchants were compared and used to determine dislocation densities.

CHAPTER 3

LITERATURE REVIEW

3.1 Point Defects

A perfect crystal is an infinite array of a basic lattice structure. The common elemental semiconductors (i.e., germanium, silicon) have a diamond lattice structure. The simplest class of bulk defects are called point defects. These are localized defects occupying a volume several angstroms on a side and are thus called zero dimensional defects. A simple point defect is an atom missing from a lattice site. The atom can be displaced to the crystal surface, to another vacated lattice site (i.e., a vacancy) or to a site between lattice points (i.e., an interstitial site).

Foreign atoms in the lattice constitute another family of point defects. These are also called chemical defects. The foreign atom can occupy a host atom lattice site (i.e., a substitutional impurity) or an interstitial site.

The individual point defects can coalesce and form point defect complexes. Complexes include divacancies (vacancy pairs), Frenkel defects (vacancy-interstitial pairs), E centers (phosphorus-vacancy pairs), and A centers (oxygen-vacancy pairs). Several vacancies may coalesce to form clusters which are nucleating sites for more complex defect structures. Foreign atoms can coalesce at high impurity concentrations and form precipitates in the lattice.

Point defects are thermodynamically stable in the lattice, a property unique among defects. Thus the equilibrium number of point defects is temperature dependent and can be predicted using Boltzmann statistics with

a known point defect activation energy. For example, at room temperature Boltzmann statistics predict approximately 10^{-20} vacancies per cm^3 of silicon while at temperatures near the melting point of silicon approximately 10^{15} vacancies per cm^3 is predicted. Silicon wafers are frequently subjected to high temperatures (i.e., crystal growth, oxide growth, diffusion) then quickly cooled, "freezing in" the vacancies and self interstitial atoms (intrinsic point defects) that were created at the high temperatures. The quenching of intrinsic point defects into the lattice results in many more vacancies and self interstitial atoms existing at room temperature than might otherwise be expected. In addition to thermal energy, the necessary activation energy can be derived from stresses in the lattice. Lattice stresses increase the crystalline free energy which can be lowered by the creation of point defects.

Point defects stress the lattice. Vacancies cause a localized collapse of the lattice around the missing atom site. Host and foreign interstitial atoms cause localized lattice expansion. Foreign substitutional atoms can either dilate or cause lattice compression depending on the relative sizes of the foreign and host atoms.

Point defects migrate about the crystal. The probability that a point defect will move can be predicted using Boltzmann statistics with an activation energy necessary for movement. A point defect can move by exchanging places with a neighboring atom or moving to an interstitial site. Substitutional atoms migrate primarily via vacancies while interstitial foreign atoms move primarily via interstitial sites. Thus interstitial foreign atom migration is not dependent on the vacancy concentration and tend to move faster than substitutional atoms.

3.2 Dislocations

A line of point defects forms a linear type of defect called a dislocation. Lattice arrangement extends radially several angstroms around the dislocation. The dislocation can be several angstroms long or may span the length of the crystal. Dislocations generally occur, along preferred crystallographic directions called slip planes, to reduce lattice stresses.

Dislocations are complex structures. There are two limiting cases; edge and screw dislocations. The edge dislocation occurs at the edge of an incomplete plane of atoms. A screw dislocation is the result of a slipped or shifted plane of atoms. The edge dislocation is composed of dangling bonds and lattice dilation and compression while a screw dislocation involves only changes in the lattice spacing.

The dislocation type and strength (magnitude of lattice rearrangement) is characterized by a pseudo-vector called the Burgers vector. The orientation of the dislocation vector and the Burgers vector indicates the dislocation type. The strength of a dislocation is related to the magnitude of the Burgers vector.

Dislocations are not thermodynamically stable and ideally crystals can be grown that are dislocation free. However, once created a dislocation is virtually a permanent structure in the lattice at room temperature. It is possible to remove dislocations using proper annealing techniques.

Elevated temperatures or lattice stresses can induce dislocation movement. This movement is characterized by two limiting cases. The simplest is glide which involves the rearrangement of atomic bonds. The other mechanism is climb which involves moving atoms as well as atomic bond rearrangement. Glide occurs parallel to the Burgers vector while climb is

perpendicular. Dislocations can grow (increase in length) via mechanisms similar to dislocation movement.

The presence of dislocations can enhance the creation of new dislocations. Dislocations can increase lattice stresses and during device fabrication these stresses may be sufficient to generate new dislocations. The processing can also cause dislocations to grow, further damaging the crystal.

Dislocations can be expanded into a planar type of defect. Planar defects include stacking faults which can be created during high temperature oxide growth and epitaxial layer growth. Further deviation from the single crystalline form create increasingly complex defects. Fortunately, the commonly encountered defects in single crystalline semiconductor grade material is limited to point defects and dislocations.

3.3 Electrical Nature of Defects

The band theory of solids is based on a regular array of closely packed identical atoms. The theory can predict the allowed electron energy states in a crystal. The amount of splitting of the allowed electron energy levels is a function of the spacing of the atoms in the crystal. This splitting of states creates the conduction band, valence band, and forbidden energy gap (band gap) in semiconductors. Any change in the regular array modifies the band structure.

Point defects introduce changes in the interatomic spacing causing localized changes in the band structure, most notably changes in the width of the band gap. Such modulation of the conduction and valence band potential can reduce carrier mobility.

Many classes of point defects contain dangling (broken or unfilled) bonds. Dangling bonds can be electrically active and may occupy energy states within the band gap. Such states can trap carriers or act as recombination centers. Dangling bonds also charge the point defect and a localized space charge region forms around the point defect to create space charge neutrality. These localized electric fields hinder carrier movement reducing carrier mobility.

Foreign substitutional atoms can increase the conductivity of the crystal. Foreign substitutional atoms with extra valence electrons that have energy states close to the conduction band (several meV) increase the number of electrons in the conduction band. Foreign substitutional atoms with deficient electron states close to the valence band capture electrons from the valence band creating more holes.

Dislocations also change the interatomic spacing, modulating the band structure around the dislocation core. The primary electrical characteristic of a screw dislocation is the band structure modulation. The electrical nature of the edge dislocation is complicated by the presence of the dangling bonds. The dangling bonds produce electronic states that may be traps or recombination centers reducing conductivity and carrier lifetime, respectively. The space charge region that forms around the edge dislocation core reduces carrier mobility. This reduction of carrier mobility, which is largely isotropic when associated with point defects, is anisotropic. Carriers moving perpendicular to the dislocation core are hindered by the space charge region. Along the dislocation core the closely spaced dangling bond wave functions overlap and create a highly conductive path along the core. The conducting pipe produces higher carrier mobility and lower

resistivity parallel to the dislocation than perpendicular to it. This lower resistivity parallel to edge dislocations is not lower than resistivity measured in similar dislocation free material. The modulation in band structure along the dislocation core also produces anisotropic changes in carrier mobility.

3.4 Diffusion Induced Damage

Intrinsic silicon presently has few uses as electrical rectifying device material. The introduction of appropriate dopant atoms into the silicon create n-type and p-type regions. Rectifying p/n junctions occur where n-type and p-type regions meet. There are various methods to introduce the dopant atoms into silicon including diffusion, ion implantation, and during epitaxial layer and crystal growth. However, in addition to doping the silicon defects are created that adversely affect conventional device performance.

Diffusion is commonly used to introduce dopant atoms into silicon. Diffusion is essentially particle movement in a solution (be it gas, liquid, or solid) via a concentration gradient. The diffusion rate is characterized by a diffusion constant or coefficient assigned to the diffusing particle in the solution. Many factors including temperature, particle concentration, and crystalline perfection affect the diffusion coefficient.

There are various types of diffusion dopant sources. Essentially all of these methods coat the semiconductor wafer with a dopant source that contains the desired impurity atoms. These include gas, vapor, solid, planar, and spin-on sources. The gas and vapor sources with appropriate carrier gases react in the diffusion tube and coat the wafer. Solid sources

are commonly sublimated or evaporated at high temperatures thereby coating the wafer. Planar sources are stacked parallel to the semiconductor wafer and at high temperature the dopant source diffuses from the planar source to the wafer. Spin-on sources are applied to the wafer prior to heating. The dopant surface concentration of gas, vapor, and spin-on sources can be controlled by adding silicon dioxide to the dopant source.

The common dopants are substitutional impurities and diffuse primarily via vacancies. At elevated temperatures there exists a higher probability of vacancy formation and substitutional atom movement (more activation energy and vacancies available). Therefore, diffusion is highly temperature dependent. At room temperature the diffusion of common dopant atoms is practically nonexistant. Consequently, diffusions are performed at high temperatures (typically $900^{o}C$ - $1200^{o}C$). But there is also a higher probability of other types of defect formation at these temperatures. The diffusion rate is also affected by the presence of these defects. For example, the severe lattice deformation along dislocation cores allow dopant atoms to diffuse very rapidly through these dislocation pipes.

Thermal gradients form if the heating of the silicon wafer is not uniform. Usually the edges of the wafer heat faster than the center and thermal gradients form creating uneven wafer expansion. Defects are formed to reduce lattice stresses and dislocations so formed span the width of the wafer. Slow wafer heating to ensure uniform heating and lower diffusion temperatures can be used to minimize defect formation.

The diffusion of substitutional impurities damages the lattice. Most of the damage is a result of the difference in size between the dopant atom and host crystal atom. Table 3.1 lists the sizes of the common dopant atoms.

The larger impurities dilate the lattice and smaller impurities induce lattice compression that create stresses which can create additional defects. Arsenic (approximately the same size as silicon) diffusions do not cause as much damage as phosphorus diffusions [23], but phosphorus is preferred because of its higher diffusivity.

TABLE 3.1

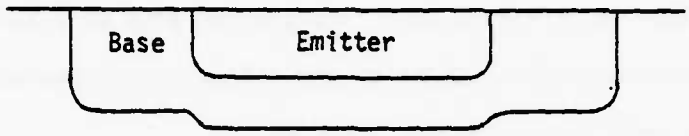
	ELEMENT	TETHRAHEDRAL RADIUS (Å)
	SILICON	1.17
N-TYPE DOPANTS:	PHOSPHORUS	1.10
	ARSENIC	1.18
P-TYPE DOPANTS:	BORON	0.88
	GALLIUM	1.26

At low concentrations lattice damage is minimal. At higher concentrations defect generation becomes evident. At still higher concentration (at the solubility limit of the dopant atoms at the diffusing conditions) defect generation due to lattice stress relief is extensive and dopant atoms tend to precipitate out of the lattice. Substitutional dopant atoms are electrically active only if located in substitutional positions. Precipitated and other off-lattice dopant atoms lower the conductivity of the diffused region [24]. If the precipitation occurs in the depletion region of a p/n junction, the precipitate concentrates the electric field and may cause premature junction breakdown.

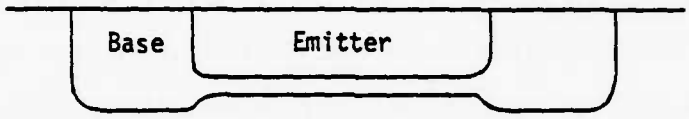
3.5 Cooperative Diffusion Effects

Simple diffusion theory assumes no interaction among the diffusing particles. It predicts a complementary error function concentration profile for undepletable dopant source diffusions (i.e., predeposition diffusion). A gaussian profile is predicted for a drive-in diffusion from an initial spike approximation predeposition diffusion. At low dopant concentrations (well below the solid solubility limit at the diffusing conditions) the concentration profile is closely approximated by the simple theory. Higher concentration profiles deviate from the theory primarily because of diffusing particle interaction. Dopant concentrations approaching saturation solubility conditions incur precipitation which also changes the concentration profile.

Double diffused structures exhibit particle interaction between different dopant species. This cooperative diffusion effect is the enhancement or retardation of the diffusion of one dopant species by the subsequent diffusion of a second dopant species. The net effect is a shift in the junction depth of double diffused structures. Enhanced diffusion of the p-type boron doped base region beneath the n-type phosphorus doped emitter is observed in npn transistors [13] [14] [15] [16] [17]. This emitter push or dip effect results in a deeper base-collector junction than expected from simple diffusion theory. Arsenic doped emitter transistors exhibit base retardation or no cooperative diffusion effects [14] [25]. Emitter push is reported in pnp transistors when the base dopant concentration is less than 4×10^{15} phosphorus atoms per cm^3 [13]. Base diffusion retardation is observed when the phosphorus base dopant concentration exceeds 4×10^{15} phosphorus atoms per cm^3. Figure 3.1 illustrates the cooperative diffusion effect in double diffused transistor structures.



Emitter Push



Base Retardation

FIGURE 3.1

Emitter regions are usually heavily doped with undersize phosphorus or boron atoms that severely stress the lattice creating defects to reduce lattice stresses. Dislocations were postulated as the emitter push mechanism until the effect was observed in dislocation free material. (Note; dislocations actually retard diffusion by absorbing vacancies [26].) It is generally agreed that a supersaturation of point defects in the base region, caused by the heavy emitter diffusion, is the source of the emitter push. There is some disagreement as to the exact nature of the point defects involved. Supersaturation of vacancies [13],[14],[15],[16],[17] and supersaturation of self interstitial atoms [27] are postulated as the enhancement mechanism.

The base diffusion retardation observed in heavier doped pnp transistor base regions is attributed to enhanced phosphorus precipitation [13]. The phosphorus precipitation is believed to occur at defect sites to reduce lattice stresses. The precipitated phosphorus atoms reduces the concentration gradient of the diffusing phosphorus atoms, producing a shallower base-collector junction.

3.6 Effect of the Base Region on Transistor Performance

The base region is the most critical area of a bipolar transistor. The quality and width of the base region affects transistor current gain and switching speed. The transistor current gain is the ratio of collector current to base current. The transistor switching speed is determined by the transistor turn on and turn off times.

Many factors increase base current, including lattice damage and contamination in the base and emitter regions and base width, consequently reducing transistor gain. Lattice damage and contamination (i.e., unwanted impurities) can create recombination centers that decrease carrier lifetime. The base recombination current can be reduced by making the injected carrier base transit time (average time necessary for a carrier to cross the base) less than the carrier lifetime. This is accomplished by minimizing lattice damage and contamination (increase lifetime) and decreasing the base width. The injected carriers in the base move via diffusion and narrowing the base will increase the gradient of the injected carriers which enhances carrier velocity and decreases the base transit time. Lattice damage in the base-collector junction depletion region can create generation centers that increases base current. This generated base current

induces an emitter current to flow without an externally applied base current.

Transistor emitters are heavily doped to affect favorable injection conditions. Under forward bias the base-emitter junction injects electrons into the base and holes into the emitter (NPN transistor). Heavy doping of the emitter relative to the base doping maximizes the injection of electrons over holes reducing the base injection current. However, the heavy emitter doping also damages the lattice increasing the base recombination current.

Transistor turn on and turn off times are related to the times necessary to build up and deplete the injected carriers in the base. The number of carriers necessary is dependent on the base width, so decreasing the base width reduces the number of carriers. The creation of recombination centers in the base reduces turn off times by enhancing base carrier depletion by recombination. However, this lower switching speed achieved by decreasing the base carrier lifetime is obtained at the expense of reduced transistor gain.

CHAPTER 4

RESULTS

4.1 Wafer Material and Emitter Spin-on Dopant Sources Used

The silicon wafers used in this study came from three sources: Boron doped p-type (100) and phosphorus doped n-type (111) wafers from Wacker-Chemitronics GMBH; phosphorus doped n-type epi wafers from Motorola Incorporated and from Epitaxy Incorporated (see Table 4.1 a-c for wafer material specifications). The three inch diameter wafers were quartered to minimize the amount of wafer material used. Spin-on SiO_2 dopant sources from two manufacturers were used in this study: Phosphorosilicafilm (PSF) and arsenosilicafilm (ASF) from Emulsitone Company and Accuspin phosphorus (P-120) and arsenic (As-120) from Allied Chemical Corporation.

The spin-on sources first used in this study were the Emulsitone sources. The PSF initially chosen reportedly produced an electrically active dopant concentration, $C_s = 5 \times 10^{20}$ phosphorus atoms per cm^3 and the ASF, $C_s = 2 \times 10^{20}$ arsenic atoms per cm^3. Mixes containing both PSF and ASF in the correct ratios were to serve as the dual dopant diffusion sources. Emulsitone chemists confirmed by telephone that the PSF and ASF solutions are meniscable and the resultant mix could be used as a dual dopant source. Our measured sheet resistances (see Appendix A for sheet resistance measurement procedure) of the PSF diffused layers were close to the manufacturer's specifications (Table 4.2a). However, our measured sheet resistances of the ASF diffused layers were much higher than the manufacturer's specifications (Table 4.2b). The sheet resistance of Emulsitone Emitter Diffusion Source N-250 diffused layers were also measured. The N-250 sources reportedly produced a $C_s = 1 \times 10^{21}$ phosphorus atoms per cm^3.

TABLE 4.1a

Wacker Material Specifications

TYPE: P-TYPE, BORON DOPED
ORIENTATION: 1-0-0
RESISTIVITY: 1.90-2.4 Ω-cm.
THICKNESS: 14.0-16.0 mils.
DIAMETER: 3.0 inches

	position on the wafer						
	1	2	3	4	5	$\overline{\rho}$	$\overline{x}$
resistivity (Ω-cm) (four point probe)	2.5	2.9	2.8	2.7	2.8	2.7	0.2

TYPE: N-TYPE, PHOSPHORUS DOPED
ORIENTATION: 1-1-1
RESISTIVITY: 5.5-11 Ω-cm.
THICKNESS: 14.0-16.0 mils.
DIAMETER: 3.0 inches

	position on the wafer						
	1	2	3	4	5	$\overline{\rho}$	$\overline{x}$
resistivity (Ω-cm) (four point probe)	9.3	9.5	9.1	9.2	9.4	9.3	0.2
	7.8	7.4	7.2	7.6	7.4	7.5	0.2

TABLE 4.1b

Motorola Material Specifications

TYPE:	n-type, phosphorus doped epi layer on n^+ substrate
ORIENTATION:	1-1-1
EPI RESISTIVITY:	14 Ω-cm.
EPI THICKNESS:	12 μm.
THICKNESS:	11 - 14 mils.
DIAMETER:	2 inches

TABLE 4.1c

Epitaxy Material Specifications

TYPE:	n-type, phosphorus doped epi layer on p substrate
ORIENTATION:	1-1-1
EPI RESISTIVITY:	2.3 Ω-cm.
EPI THICKNESS:	12.5 μm.
THICKNESS:	14 mils.
DIAMETER:	3 inches

TABLE 4.2a

PSF, $C_s = 5 \times 10^{20}$, Sheet Resistance Measurements (Ω/square)

process	Wacker wafer used	position on the wafer 1	2	3	4	5	$\overline{\rho_s'}$	$\bar{x}$	published $\overline{\rho_s'}$
20 min. at 1050°C	n-type	6.1	6.2	6.3	6.3	6.7	6.3	0.2	5
1 hr. at 950°C	n-type	7.1	7.2	7.4	7.2	7.3	7.2	0.1	-
1 hr. at 1050°C	n-type	4.9	5.1	4.9	4.9	4.8	4.9	0.1	-
1 hr. at 1050°C	p-type	4.9	5.0	5.3	4.9	5.1	5.0	0.2	-

TABLE 4.2b

ASF, $C_s = 2 \times 10^{20}$, Sheet Resistance Measurements (Ω/square)

process	Wacker wafer used	position on the wafer 1	2	3	4	5	$\overline{\rho_s'}$	$\bar{x}$	published $\overline{\rho_s'}$
1 hr. at 1150°C	n-type	41.9	44.2	45.0	40.2	43.4	42.9	1.9	13
1 hr. at 1150°C	p-type	64.7	73.7	88.5	59.8	67.1	70.8	11.1	13

TABLE 4.2c

N-250, $C_s = 1 \times 10^{21}$, Sheet Resistance Measurements (Ω/square)

process	Wacker wafer used	position on the wafer 1	2	3	4	5	$\overline{\rho_s'}$	$\overline{x}$	published $\overline{\rho_s'}$
1 hr. at 1150°C	n-type	3.2	3.5	3.4	3.4	3.3	3.4	0.1	4.2
1 hr. at 1150°C	p-type	3.3	3.4	3.8	3.3	3.4	3.4	0.2	4.2

Arsenic is also present in the N-250 source in the ratio of 3.7 phosphorus atoms per arsenic atom. Emulsitone claims the arsenic in the N-250 source at the aforementioned phosphorus to arsenic ratio compensates the lattice strain caused by the high concentration phosphorus diffusion. Our measured sheet resistance of N-250 diffused layers were lower than the manufacturer's specifications (Table 4.2c). Our measured sheet resistances of PSF and N-250 diffused layers were relatively uniform while there was some divergence for those of the ASF diffused layers.

Several wafers exhibited what appeared to be particle swirls remaining on the wafer surface after the Emulsitone spun-on glass was removed following the predeposition diffusion. Intense side lighting of the wafer surface with a microscope light revealed a nonuniform cloudy white surface where the spun-on glass was removed. In those instances where particle swirls were visible, these swirls appeared brownish with the side lighting. Optical microscopic examination of the wafer surfaces using epi-illumination revealed a featureless surface. The surface structures were initially assumed to be insoluble residue from the spun-on glass and attempts to clean the wafer surface (see Appendix B for wafer cleaning procedure) succeeded in only removing the swirls. Emulsitone claims their PSF and ASF spin-on dopants do not produce insoluble residue or texture the silicon surface. The origin and nature of the cloudy white surface areas is not clear at this time.

The Accuspin phosphorus spin-on dopant source that reportedly produced a $C_s = 6 \times 10^{20}$ phosphorus atoms per cm^3 was tested to determine if a similar surface problem existed with the Accuspin source. Accuspin chemists also foresaw no problem mixing their P-120 and the arsenic counterpart As-120 and the resultant mix could be used as a dual dopant source. Our measured

sheet resistances of the P-120 diffused layers were lower than the manufacturer's specifications (Table 4.3). The wafer surface was inspected after the P-120 spun-on glass was removed following the predeposition diffusion using the side lighting technique and optical microscopy (with epi-illumination) and was found to be free of particle swirls and cloudy areas.

TABLE 4.3

process	Wacker wafer used	position on the wafer 1	2	3	4	5	$\overline{\rho_s'}$	$\overline{x}$
1 hr. at 950°C	n-type	31.7	33.6	32.4	32.0	32.3	32.3	0.7
1 hr. at 950°C	p-type	31.9	35.0	32.6	33.3	33.4	33.2	1.2

published sheet resistance for 1 hr. at 950°C is 39 Ω/square

4.2 Transistor Gain Measurement Tests

Simple transistor structures with common base and common collectors (Figure 4.1) were fabricated to help determine if the effects of the simultaneous diffusions could be monitored by transistor electrical characteristics. The simple transistor structure was designed to minimize fabrication

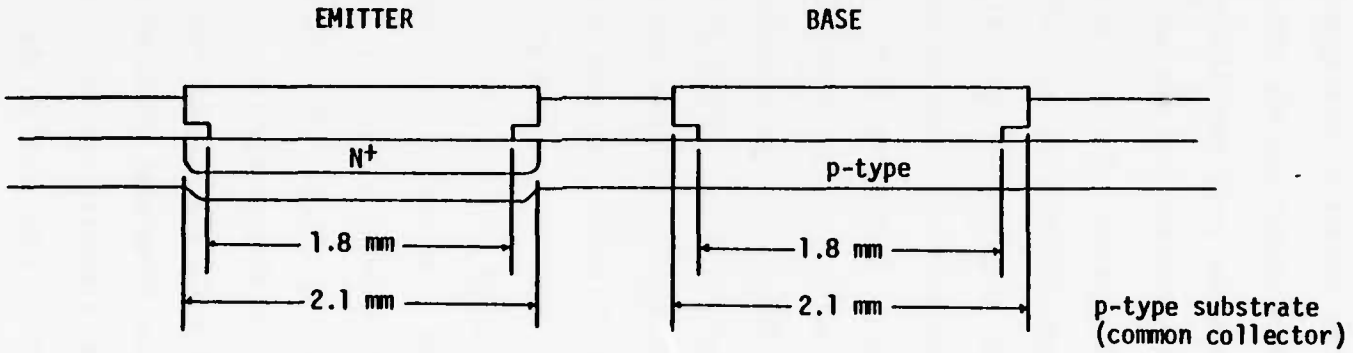


FIGURE 4.1

Cross Sectional View of the Simple Transistor Structure

time. The entire surface of an n-type Wacker wafer was doped with boron from boron nitride planar sources (see Appendix C for base diffusion schedule) to form the transistor base region. Our calculated total diffused boron concentration from the boron nitride planar source base predeposition diffusion was 1.4×10^{15} boron atoms per cm^3 which is lower than the reported [3] critical total diffused boron concentration of 1.6×10^{16} boron atoms per cm^3 for dislocation free boron diffusions. Thus dislocation generation from the boron base diffusion in our study should be minimal. The emitter diffusion windows were defined in the base drive-in oxide using a 2.1 mm. diameter dot mask. The emitters were diffused from the PSF source (see Appendix C for emitter diffusion schedule). Windows were defined in the emitter drive-in oxide using 1.8 mm. diameter dot masks to contact the base and emitter regions. The wafers were then metallized, metallization patterned using the 2.1 mm. diameter dot masks, and sintered to provide ohmic base and emitter contacts. The backside of the wafer was lapped with 600 grit silicon carbide and contacted with wire and silver paint to provide a quasi-ohmic collector contact. The wafer was scribed around the edges to minimize possible wafer edge carrier recombination and shorting effects. The simple transistor structures exhibited unusual electrical characteristics (Figures 4.2 a-c). Both the base-emitter (Figure 4.2b) and base-collector (Figure 4.2c) junctions of the simple transistor structures exhibited very high leakage currents.

The unusual electrical characteristics of the simple transistor structures was initially attributed to the PSF spin-on dopant source. Diodes were fabricated by diffusing phosphorus from the PSF batch used for the simple transistor structures and from an older batch of PSF (both PSF batches reportedly produced the same C_s) into p-type Wacker wafers to test

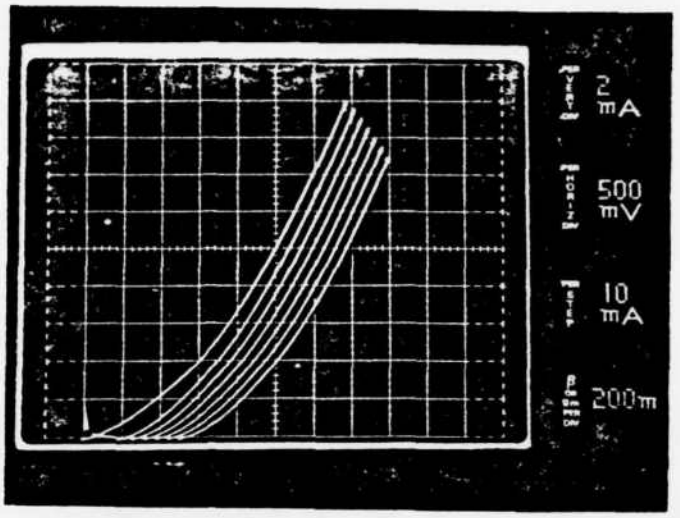
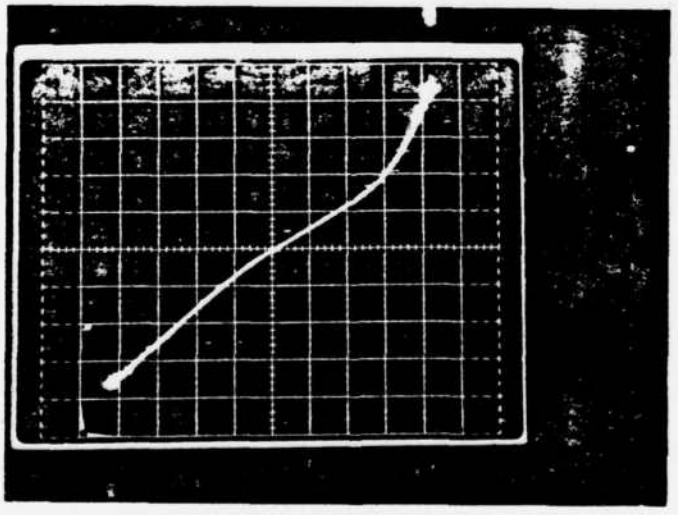


FIGURE 4.2a

Simple Transistor I_c-V_{ce} Characteristics

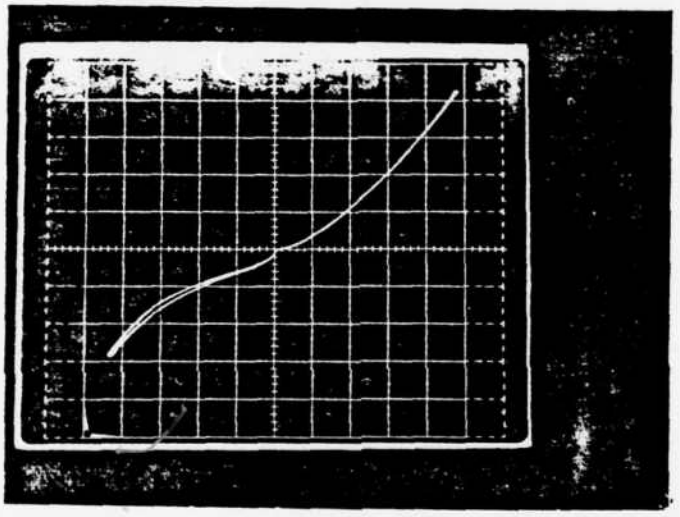


Forward Bias:
2 mA/div.
200 mV/div.

Reverse Bias:
20 mA/div.
2 V/div.

FIGURE 4.2b

Simple Transistor Base-Emitter Junction Characteristics



Forward Bias:
2 mA/div.
500 mV/div.

Reverse Bias:
20 mA/div.
20 V/div.

FIGURE 4.2c

Simple Transistor Base-Collector Junction Characteristics

the PSF spin-on sources. A one hour predeposition diffusion at 1100°C was used to create the phosphorus doped n-type regions. These diodes, fabricated with the dot masks, were then metallized, metallization patterned, and sintered. The diodes were tested (back to back diodes) and both sets of diodes exhibited excellent reverse biased junction characteristics with sharp junction breakdown and low leakage currents (Figures 4.3 a,b). The excellent reverse bias characteristics indicate that the PSF spin-on dopant was not the cause of the simple transistor structures' unusual electrical characteristics and that the cause was elsewhere (such as a result of the simple transistor structure, bad n-type wafers, or a processing error).

It was assumed that the n-type Wacker material was not the source of the simple transistor structures' unusual electrical characteristics and were used to fabricate another, more conventional transistor structure (Figures 4.4 a-g). Similar transistors had been previously fabricated by Sinthavone Soutavong (a former graduate student) in the solid state device laboratory. Sinthavone's transistors exhibited good transistor characteristics with gains in excess of 300 and were fabricated using boron nitride planar sources for the base diffusion and P_2O_5 glass source from PH_3 gas for the emitter diffusion. Our transistors were fabricated using the same schedule as Sinthavone's transistors (see Appendix C for fabrication schedule) except PSF with $C_s = 5 \times 10^{20}$ phosphorus atoms was used as the emitter diffusion source in our transistors. This transistor fabrication schedule was chosen because it represents a "textbook", generallized type of transistor [23]. Figures 4.5 a,b are photographs of typical conventional transistors fabricated for our study. The PSF/Wacker transistors exhibited good electrical characteristics (Figures 4.6 a-c) with gains as

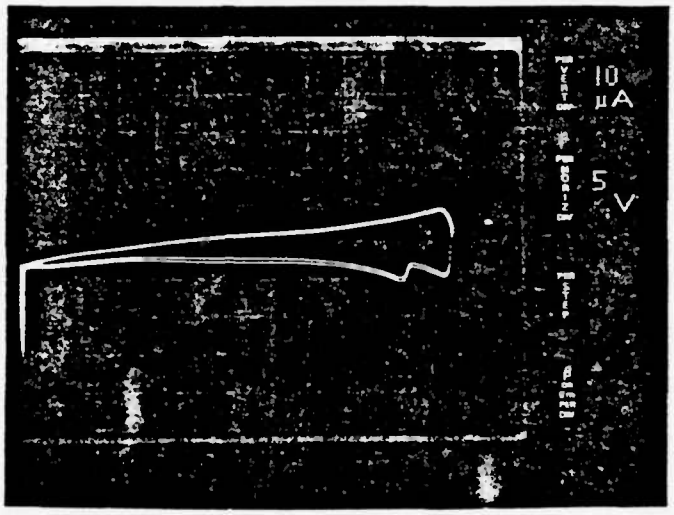


FIGURE 4.3a

Old PSF Diode Reverse Bias Characteristics

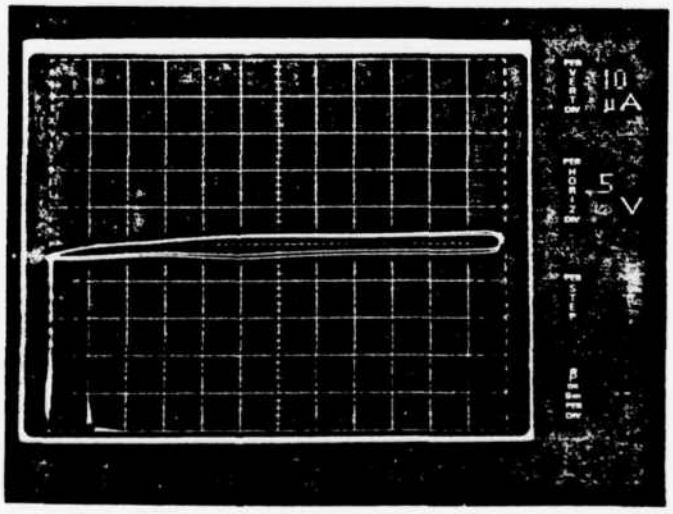


FIGURE 4.3b

New PSF Diode Reverse Bias Characteristics

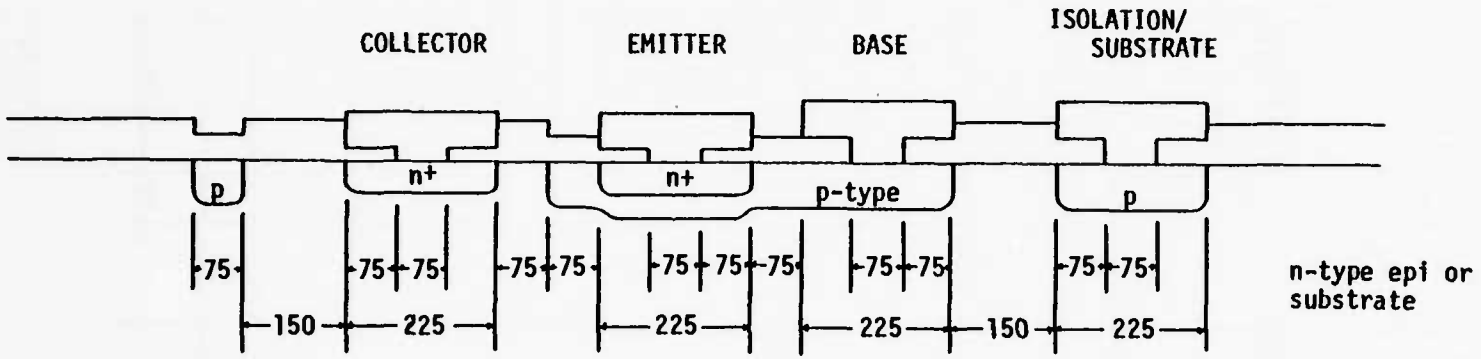


FIGURE 4.4a

Cross Sectional View of the Conventional Transistor Structure
(Junction depths, oxide and metal thickness are not to scale)
(Dimensions in micrometers)

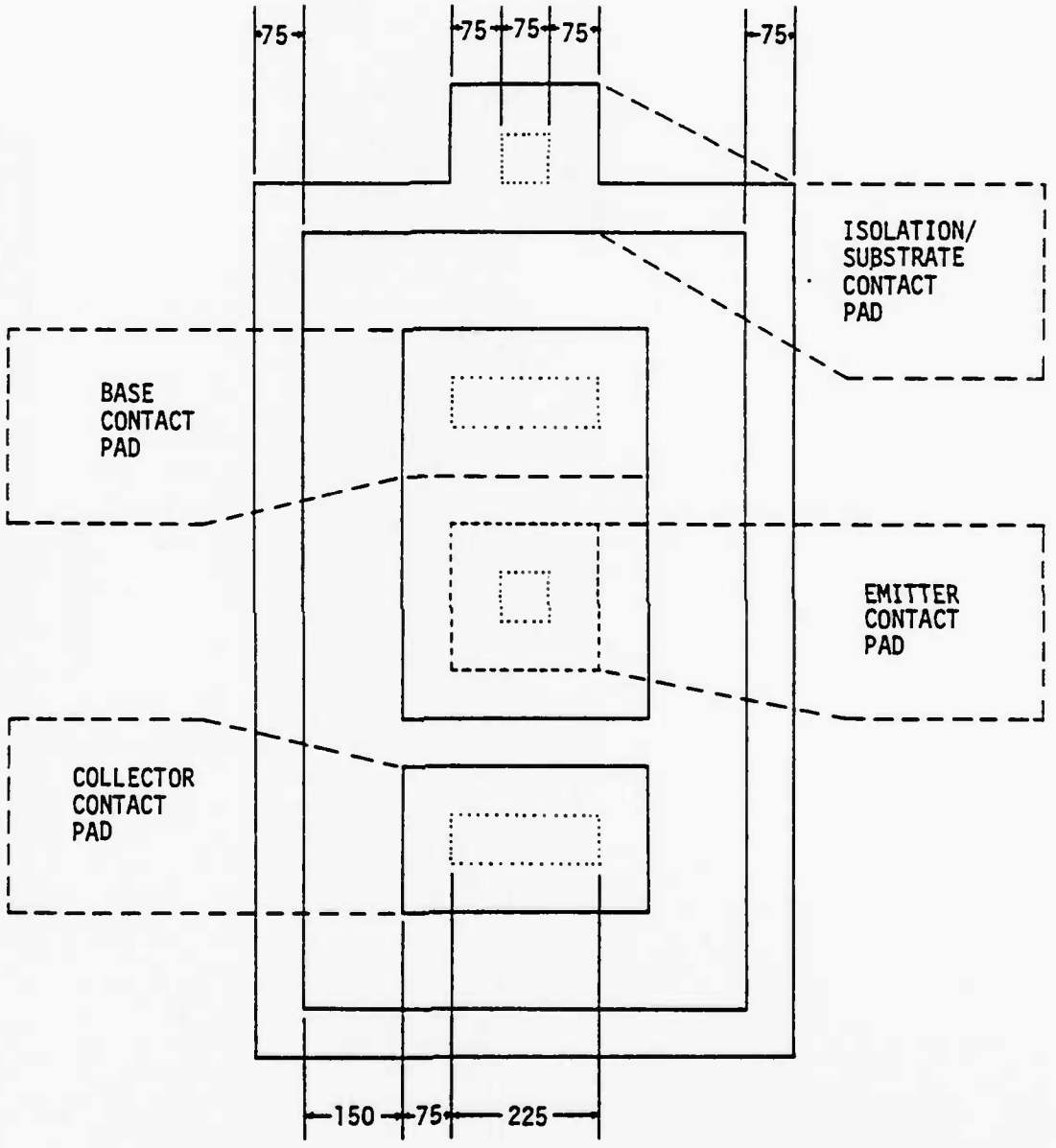


FIGURE 4.4b

Top View of the Conventional Transistor Structure
(Dimensions in micrometers)

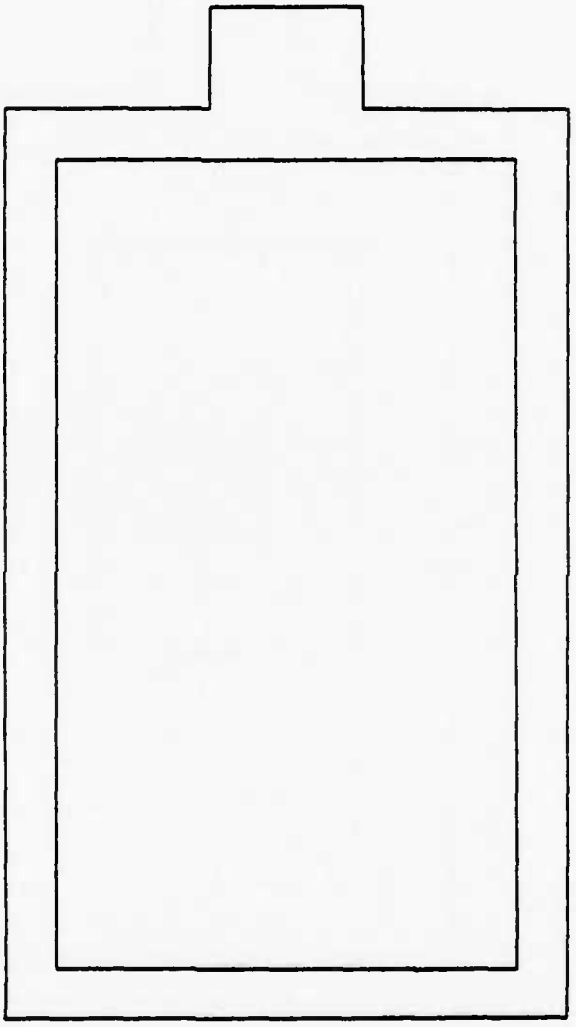


FIGURE 4.4c

Isolation Definition Mask

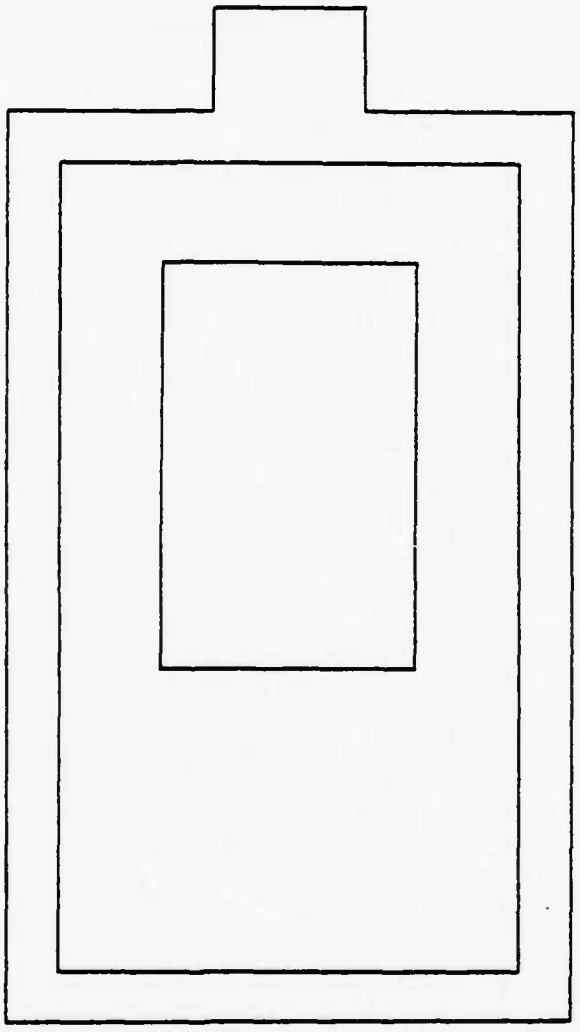


FIGURE 4.4d

Base Definition Mask

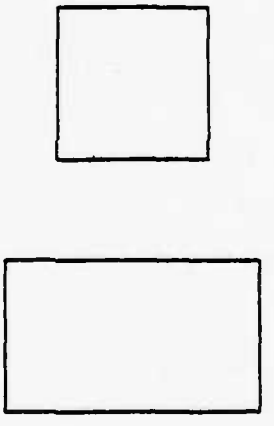


FIGURE 4.4e

Emitter Definition Mask

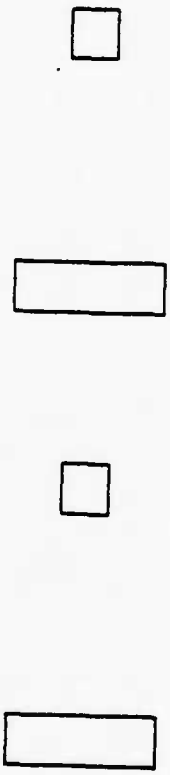


FIGURE 4.4f

Contact Window Definition Mask

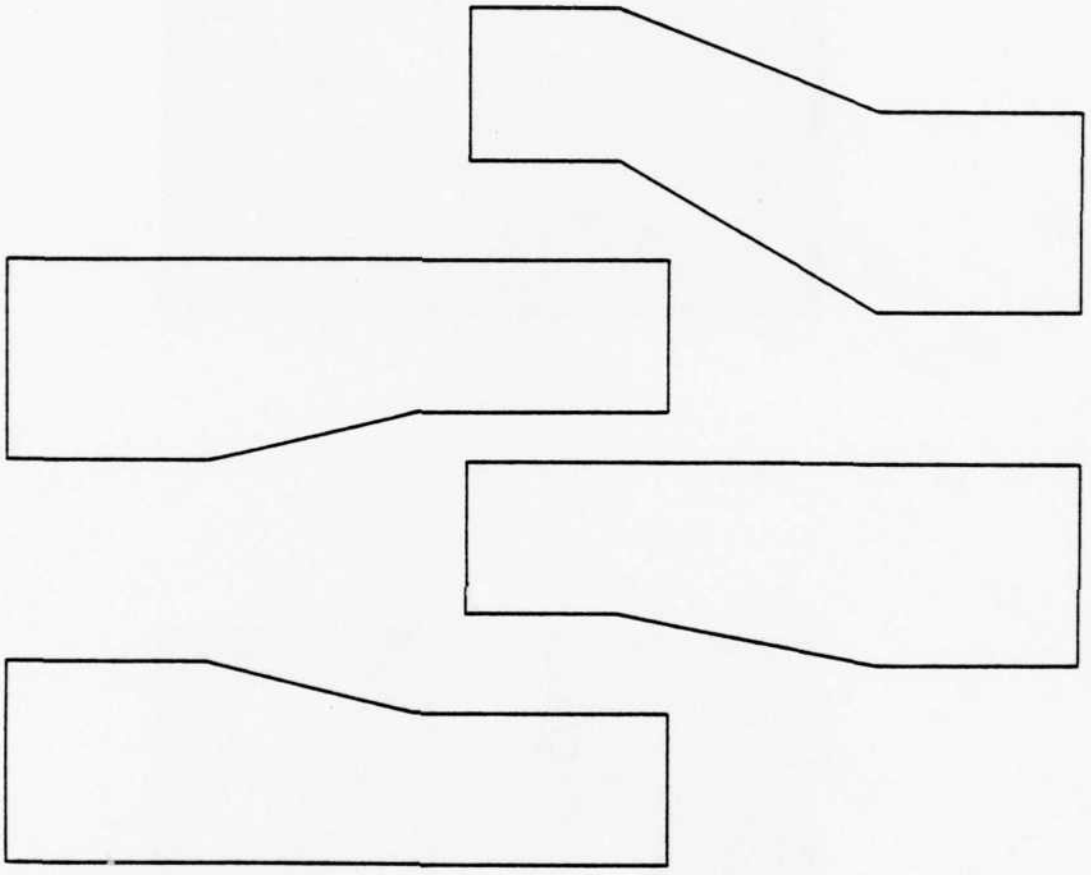


FIGURE 4.4g

Metallization Definition Mask

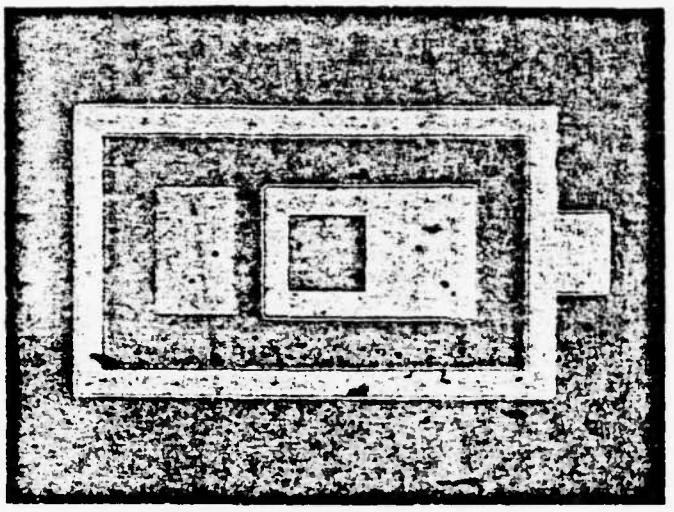


FIGURE 4.5a

Photomicrograph of Unmetallized Transistor

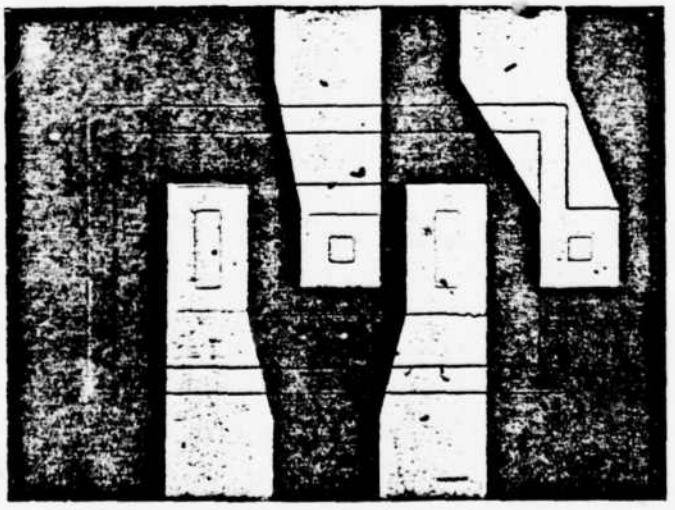


FIGURE 4.5b

Photomicrograph of Completed Transistor

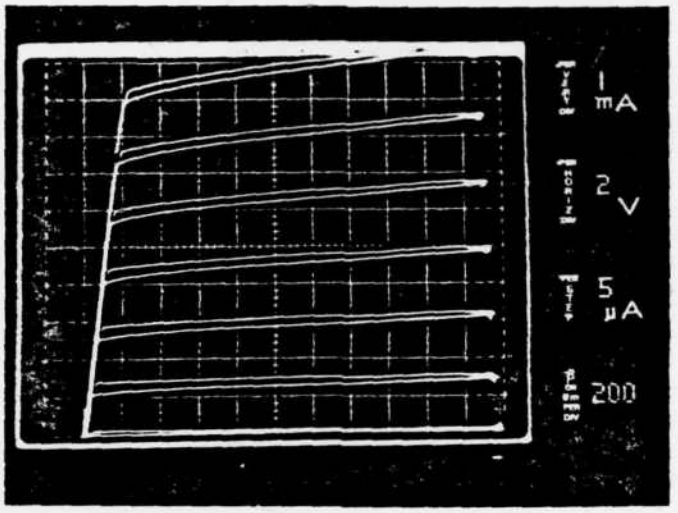
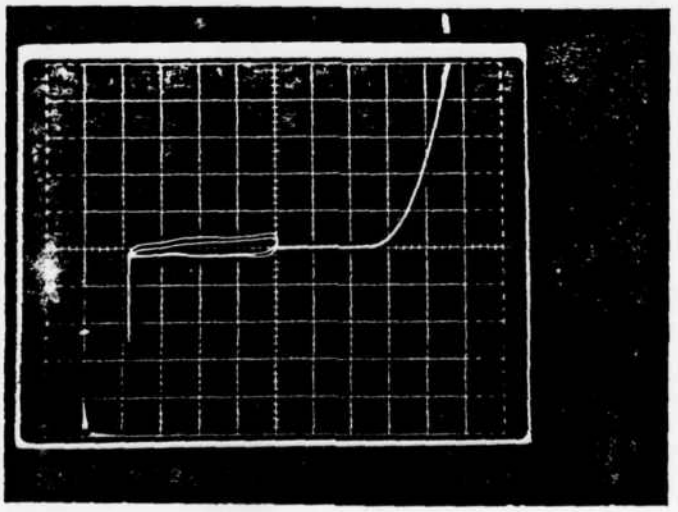


FIGURE 4.6a

PSF/Wacker Transistor I_c-V_{ce} Characteristics

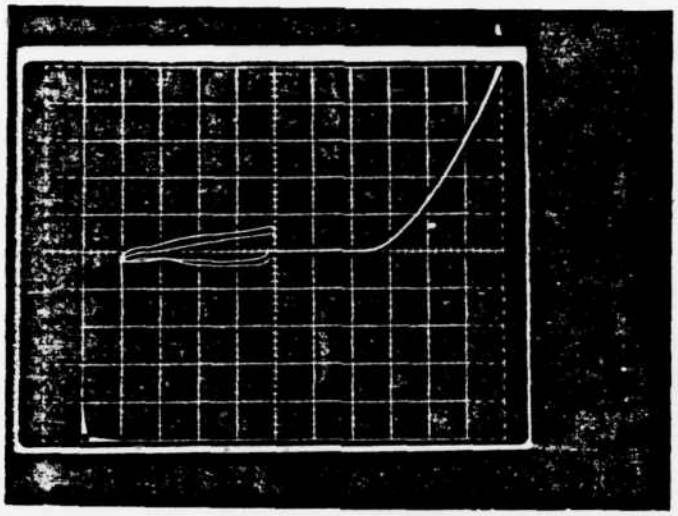


Forward Bias:
1 mA/div.
200 mV/div.

Reverse Bias:
1 μA/div.
2 V/div.

FIGURE 4.6b

PSF/Wacker Transistor Base-Emitter Junction Characteristics



Forward Bias:
1 mA/div.
200 mV/div.

Reverse Bias:
5 μA/div.
20 V/div.

FIGURE 4.6c

PSF/Wacker Transistor Base-Collector Junction Characteristics

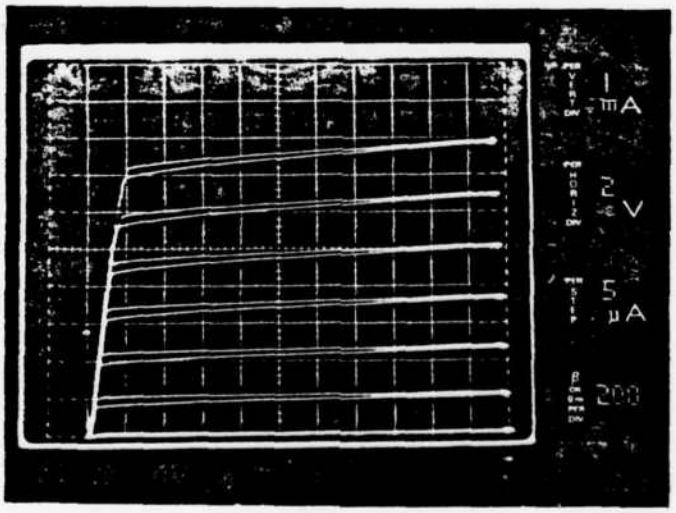
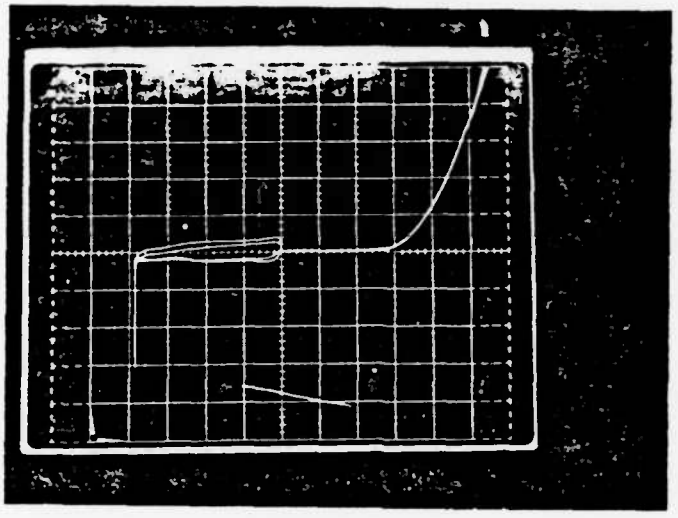


FIGURE 4.6d

PSF/Wacker, "tuned up" Transistor I_c-V_{ce} Characteristics

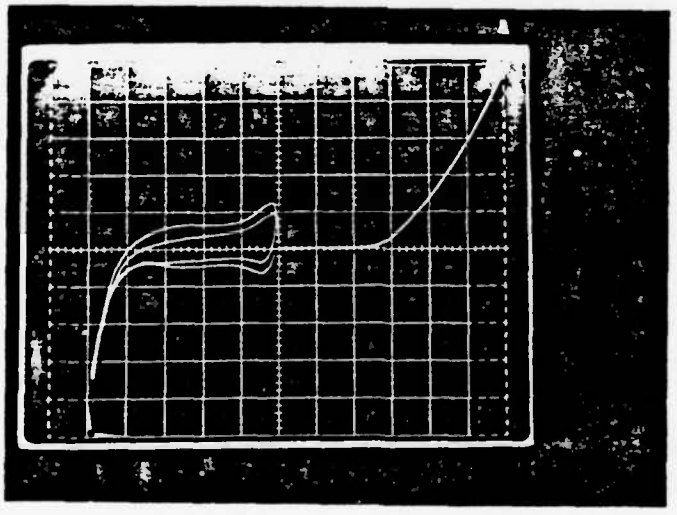


Forward Bias:
2 mA/div.
200 mV/div.

Reverse Bias:
1 μA/div.
2 V/div.

FIGURE 4.6e

PSF/Wacker, "tuned up" Transistor Base-Emitter Junction Characteristics



Forward Bias:
1 mA/div.
200 mV/div.

Reverse Bias:
2 μA/div.
10 V/div.

FIGURE 4.6f

PSF/Wacker, "tuned up" Transistor Base-Collector Junction Characteristics

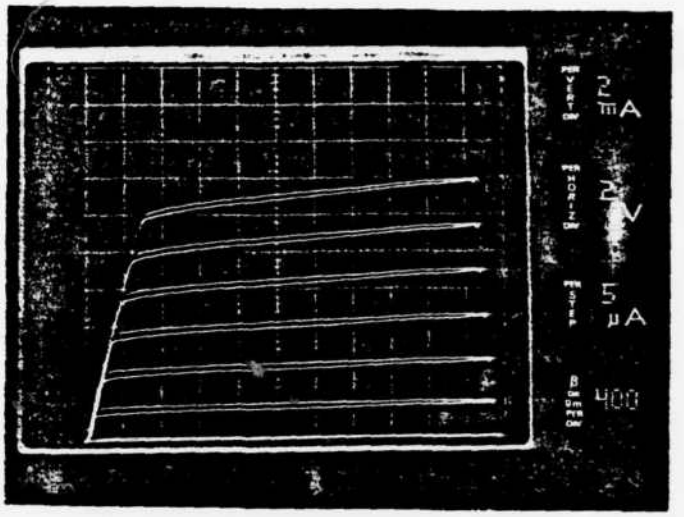
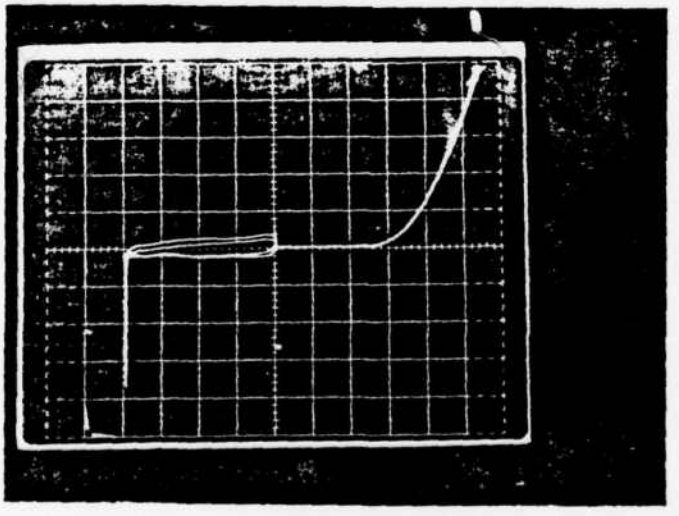


FIGURE 4.6g

N-250/Wacker Transistor I_c-V_{ce} Characteristics

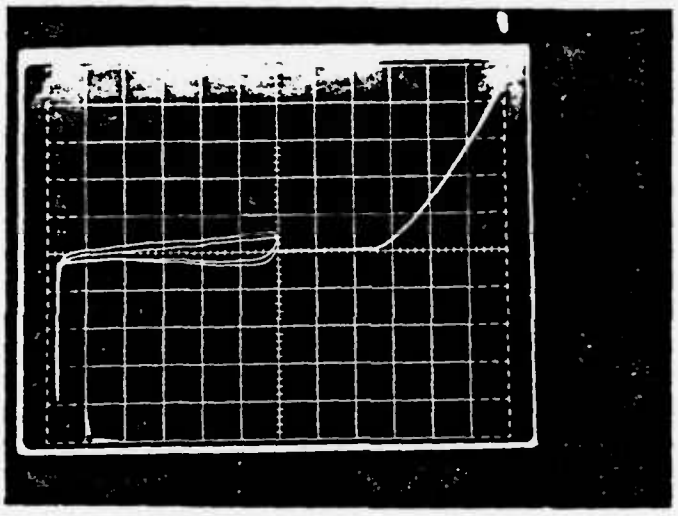


Forward Bias:
2 mA/div.
200 mV/div.

Reverse Bias:
1 µA/div.
2 V/div.

FIGURE 4.6h

N-250/Wacker Transistor Base-Emitter Junction Characteristics



Forward Bias:
1 mA/div.
200 mV/div.

Reverse Bias:
5 μA/div.
10 V/div.

FIGURE 4.6i

N-250/Wacker Transistor Base-Collector Junction Characteristics

high as 300. However, the gain was not uniform from transistor to transistor across the wafer. Neighboring transistors exhibited gains varying from 50 to 300. The base-emitter (Figure 4.6b) and base-collector (Figure 4.6c) junctions of the PSF/Wacker transistors exhibited good diode characteristics with sharp junction breakdown and low leakage current.

The transistor gains were increased by lengthening the emitter drive-in diffusion time by an additional half hour. These "tuned up" PSF/Wacker transistors also exhibited good electrical characteristics (Figures 4.6 d-f) with gains as high as 400. Wide variations in transistor gains were again observed.

Conventional transistors were also fabricated using the N-250 emitter diffusion source in place of the PSF. The N-250 transistors also exhibited good electrical characteristics (Figures 4.6 g-i) and good but widely varying gains (excess of 400).

Conventional transistors were fabricated using P-120 for the emitter dopant source in n-type Wacker wafers (see Appendix C for fabrication schedule). The P-120/Wacker transistors exhibited good electrical characteristics (Figures 4.7 a-c) but the transistor gains (ranging from 2 to 10) were substantially lower than the previously fabricated PSF/Wacker transistors. The base-emitter junctions (Figure 4.7b) of the P-120/Wacker transistors displayed "soft" junction breakdown characteristics.

Uniform transistor electrical characteristics are needed in order to use this method to monitor the effects of the simultaneous diffusions. The variation in the wafer resistivity (Table 4.1) was suspected as a source of the gain nonuniformity. Epitaxially deposited layers should have more uniform sheet resistances, so conventional transistors were fabricated in n-type epi-wafers from Motorola using P-120 for the emitter dopant

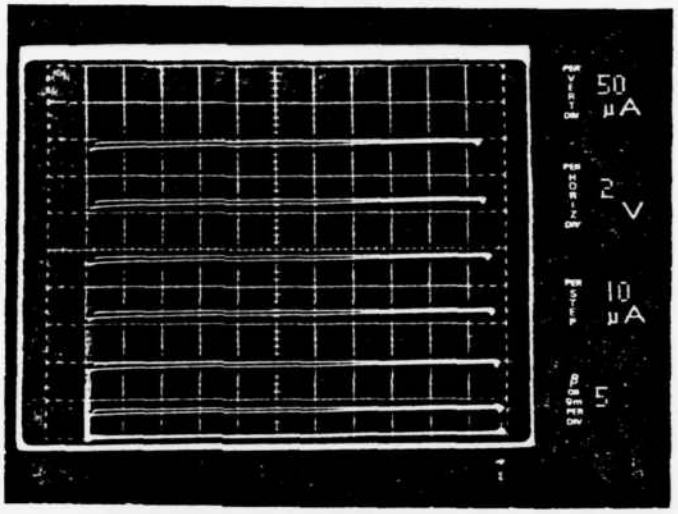
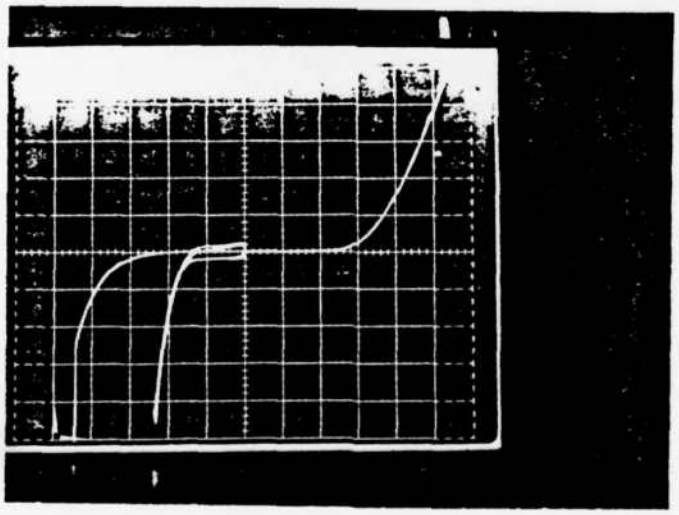


FIGURE 4.7a

P-120/Wacker Transistor I_c-V_{ce} Characteristics

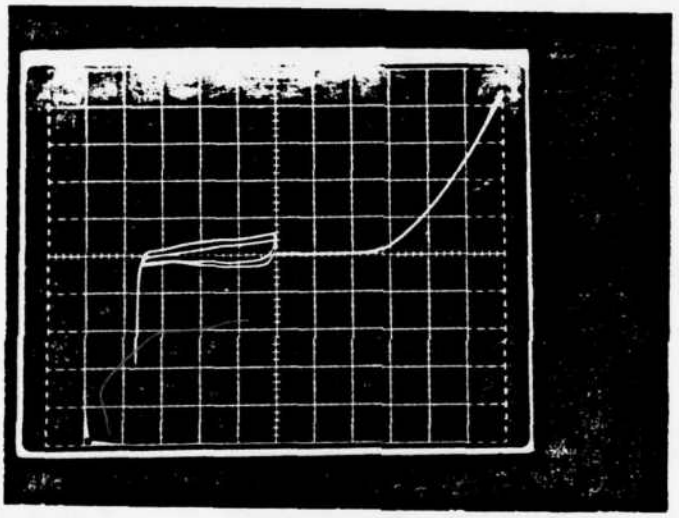


Forward Bias:
1 mA/div.
200 mV/div.

Reverse Bias:
1 A/div.
lower trace
100 A/div.
upper trace
2 V/div.

FIGURE 4.7b

P-120/Wacker Transistor Base-Emitter Junction Characteristics



Forward Bias:
1 mA/div.
200 mV/div.

Reverse Bias:
5 μA/div.
20 V/div.

FIGURE 4.7c

P-120/Wacker Transistor Base-Collector Junction Characteristics

source. Attempts to measure the epi-layer sheet resistance using the four point probe technique (see Appendix A for procedure) failed, possibly due to the thinnest and high resistivity of the epi-layer. The P-120/Motorola transistors exhibited gains (ranging from 0.5 to 4) that were lower than the previously fabricated P-120/Wacker transistors and no improvement in gain uniformity. The base-emitter junctions (Figure 4.8b) of the P-120/Motorola transistors exhibited very "soft" junction breakdown characteristics, similar to the base-emitter junctions of the P-120/Wacker transistors (Figure 4.7b).

It was initially assumed that the P-120 emitter diffused transistors would exhibit larger gains than PSF emitter diffused transistors because of the reported higher P-120 dopant surface concentration. A higher emitter surface dopant concentration should produce a deeper base-emitter junction, decreasing the base width thereby increasing transistor gain (assuming other factors remain constant). However, the P-120 emitter diffused transistors consistently exhibited lesser gains than the lower dopant surface concentration PSF emitter diffused transistors. An inspection of sheet resistance measurements from similar diffusing conditions (1 hour at a $50^{o}C$) revealed that the P-120 diffused layers had a sheet resistance that was almost five times that of PSF diffused layers. The higher sheet resistances of diffused layers from P-120 indicated that the P-120 source may have produced a shallower base-emitter junction and consequently wider base than the PSF source, thereby causing the P-120 emitter diffused transistors to exhibit lower gains than PSF emitter diffused transistors.

A modification of the transistor fabrication schedule was made to attempt to increase P-120 emitter diffused transistor gains. The modification lowered the base drive-in diffusion temperature (see Appendix C for

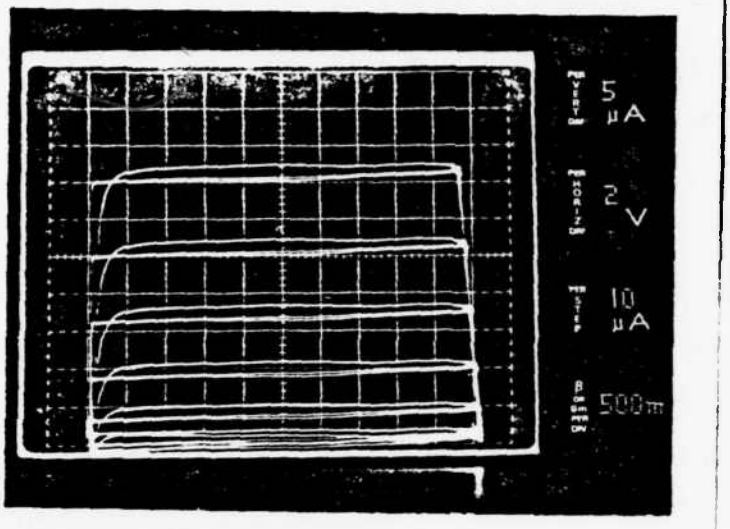
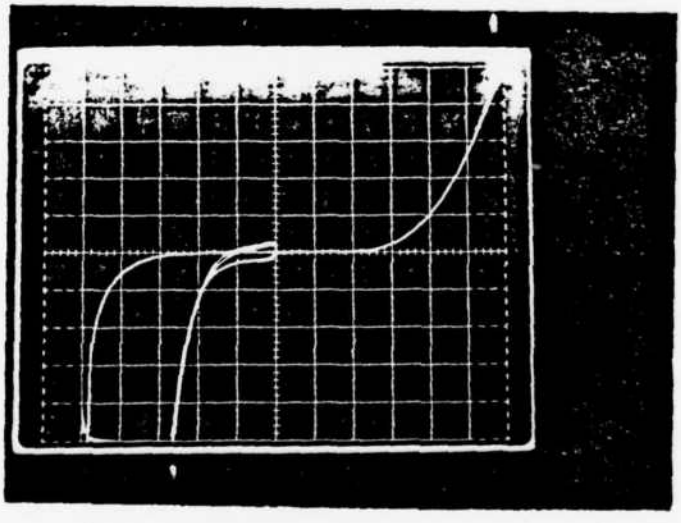


FIGURE 4.8a

P-120/Motorola Transistor I_c-V_{ce} Characteristics

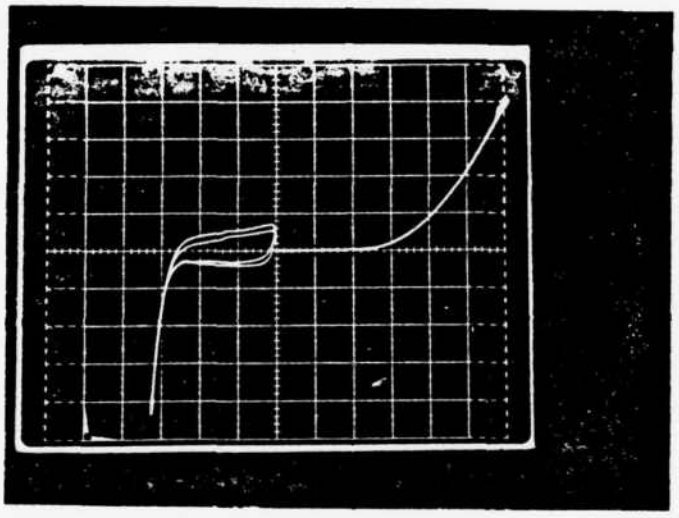


Forward Bias:
1 mA/div.
200 mV/div.

Reverse Bias:
1 µA/div.
lower trace
100 µA/div.
upper trace
2 V/div.

FIGURE 4.8b

P-120/Motorola Transistor Base-Emitter Junction Characteristics



Forward Bias:
1 mA/div.
200 mV/div.

Reverse Bias:
5 μA/div.
20 V/div.

FIGURE 4.8c

P-120/Motorola Transistor Base-Collector Junction Characteristics

fabrication schedule) from 1150°C to 1100°C to decrease the depth of the base-collector junction. The modified schedule conventional structure transistors were fabricated in n-type epi-wafers from Epitaxy because a larger stock of Epitaxy wafer material was readily available. Again, the attempts to measure the epi-layer sheet resistance using the four point probe technique failed. Although the modified schedule P-120/Epitaxy transistor gains were larger than those of the P-120/Motorola transistors, the gains were still substantially lower than those of the PSF/Wacker transistors. The junction characteristics of the modified schedule P-120/Epitaxy transistors (Figures 4.9 b,c) were similar to those of the P-120/Motorola and P-120/Wacker transistors.

Several transistors of each of the conventional structure transistors set fabricated were lapped and stained to measure the amount of emitter push caused by the spin-on sources (Table 4.4). The emitter push from the PSF source was quite significant (5000 - 6000 Å). The amount of emitter push from the N-250 source was similar to the amount from the PSF source. However, the surface phosphorus concentration of the N-250 source is twice that of the PSF source and the base-emitter junction depth from the N-250 source was significantly deeper (~ 8000 Å deeper) than from the PSF source. The preceding observations indicated that the arsenic present in the N-250 source may be reducing emitter push. There was no emitter push from the P-120 source which is possibly due to the shallowness of the P-120 source base-emitter junction.

The increase in gain of the "tuned up" PSF/Wacker transistors and modified schedule P-120/Epitaxy transistors were accompanied by a decrease in base width. This indicated that gain measurements are sensitive to possible simultaneous diffusion effects on emitter push.

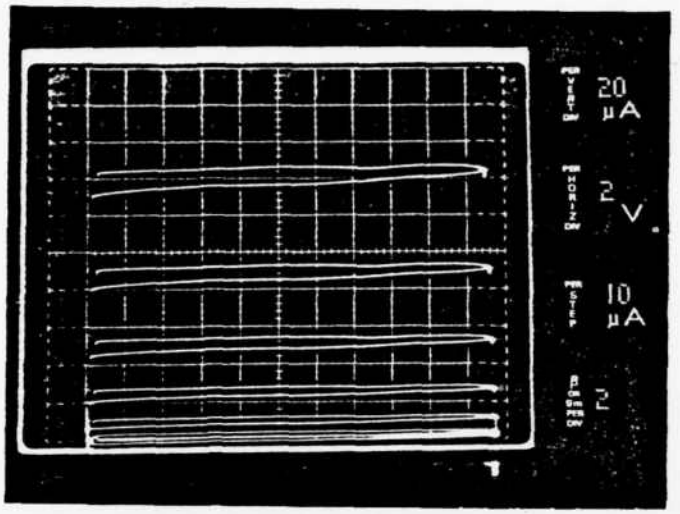
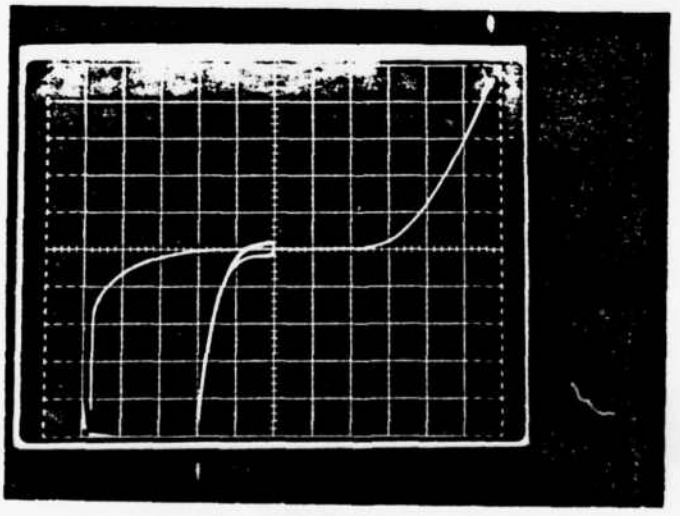


FIGURE 4.9a

P-120/Epitaxy Transistor I_c-V_{ce} Characteristics

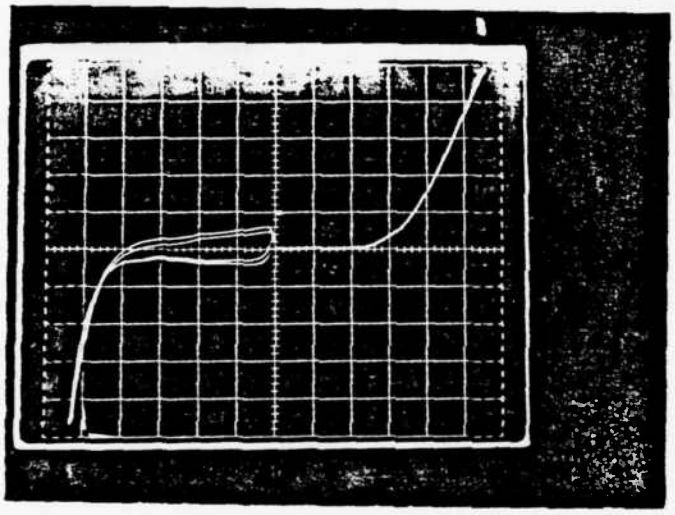


Forward Bias:
1 mA/div.
200 mV/div.

Reverse Bias:
1 μA/div.
lower trace
100 μA/div.
upper trace
2 V/div.

FIGURE 4.9b

P-120/Epitaxy Transistor Base-Emitter Junction Characteristics



Forward Bias:
500 μA/div.
200 mV/div.

Reverse Bias:
5 μA/div.
10 V/div.

FIGURE 4.9c

P-120/Epitaxy Transistor Base-Emitter Junction Characteristics

TABLE 4.4

Lap and Stain Measurements (μm)

Transistor Set	Emitter	Base	Push	Base Width
PSF/Wacker	2.1	3.4	0.5	1.8
	2.1	3.3	0.7	1.2
PSF/Wacker, "tuned up"	2.3	3.6	0.5	1.8
	2.4	3.5	0.5	1.6
	2.7	3.5	0.5	1.3
	2.8	3.4	0.6	1.2
	2.7	3.5	0.7	1.5
	2.7	3.4	*	-
N-250/Wacker	2.7	3.6	0.5	1.4
	2.7	3.5	0.5	1.3
	3.0	3.5	0.6	1.1
	3.0	3.6	*	-
	2.8	3.6	*	-
	2.8	3.6	0.6	1.4

*bad junction delineation

TABLE 4.4 (continued)

Transistor Set	Emitter	Base	Push	Base Width
P-120/Wacker	1.2	4.0	0	2.8
P-120/Motorola	0.7	3.7	0	3.0
P-120/Epitaxy	0.7	2.1	0	1.4
	1.2	2.3	0	1.1

As suspected, the P-120 emitter diffused transistors had shallower emitters and wider base regions than the PSF emitter diffused transistors. Although the modified transistor fabrication schedule succeeded in halving the base width of the P-120 emitter diffused transistors and a consistent increase in gain was noticed (halving the base width, assuming short base conditions, would ideally double the gain), there still existed a significant difference in gain between the P-120/ Epitaxy and PSF/Wacker transistors. The preceding observation indicated that the solution to increasing the gain of P-120 emitter diffused transistors required much more work.

It was decided to use PSF instead of P-120 for the emitter diffusion source (since the P-120 emitter diffused transistors had failed to produce high gain, uniform gain, and show emitter push) to minimize additional development work to produce uniform gain transistors. Although there were cloudy areas on the silicon surface after the PSF glass was removed, the PSF emitter diffused transistors exhibited high gain and emitter push. Also, the cloudy areas had no apparent deleterious effect on oxide growth.

Conventional transistors were fabricated in Epitaxy wafers using PSF for the emitter dopant source (see Appendix C for fabrication schedule). The PSF/Epitaxy transistors exhibited low gains and collector current with no applied base current (Figure 4.10a). Both junctions of the PSF/Epitaxy transistors (Figures 4.10 b,c) had high leakage currents. The base-collector junction (Figure 4.10c) showed a significant increase in leakage current compared to previously fabricated transistors. This high base-collector junction current is possibly the source of the "internal" base current that caused the collector current to flow with no applied base current. Furnace contamination or processing error were suspected as causes of the significant increase in leakage current.

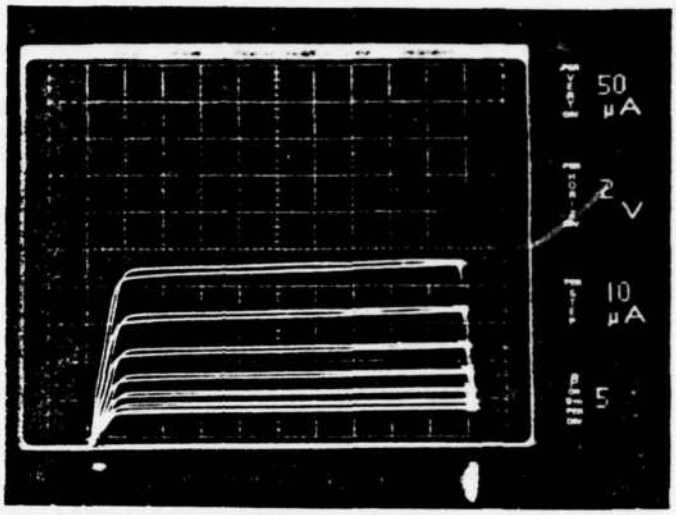
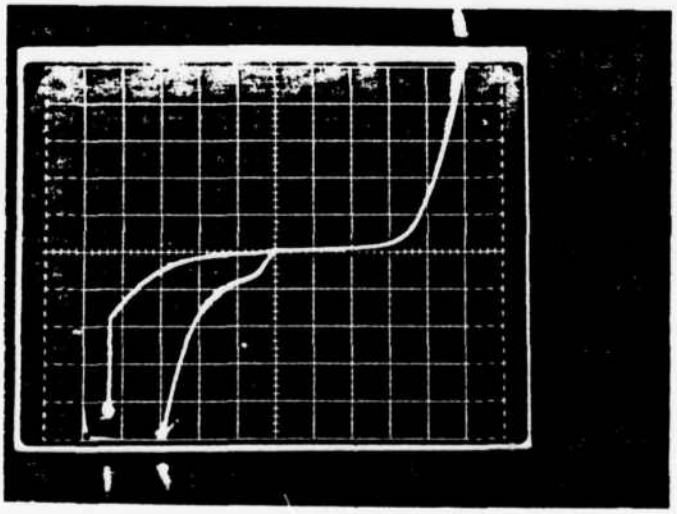


FIGURE 4.10a

First Set PSF/Epitaxy Transistor I_c-V_{ce} Characteristics

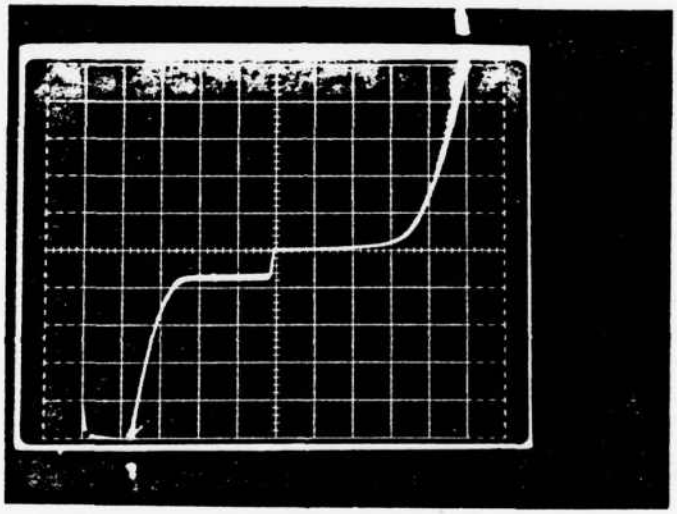


Forward Bias:
2 mA/div.
200 mV/div.

Reverse Bias:
50 μA/div.
lower trace
500 μA/div.
upper trace
2 V/div.

FIGURE 4.10b

First Set PSF/Epitaxy Transistor Base-Emitter Junction Characteristics



Forward Bias:
2 mA/div.
200 mV/div.

Reverse Bias:
50 μA/div.
10 V/div.

FIGURE 4.10c

First Set PSF/Epitaxy Transistor Base-Collector Junction Characteristics

Diodes were fabricated, using boron nitride planar sources, in both Epitaxy and n-type Wacker wafers to test for furnace contamination. The diffusion schedule used was the same as for the transistor base diffusion (see Appendix C for fabrication schedule). Both Epitaxy and Wacker diodes exhibited low leakage current and "soft" breakdown characteristics (Figures 4.11 a,b). Comparison with the first diodes fabricated (Figures 4.3 a,b) showed a degradation in diode characteristics, indicating slight furnace contamination. However, the high base-collector junction leakage current in the PSF/Epitaxy transistors did not reappear, indicating that furnace contamination was not the principal cause of the high leakage current.

Another set of conventional transistors were fabricated in both Epitaxy and Wacker wafers using PSF for the emitter diffusion source (see Appendix C for fabrication schedule). This second set of PSF/Epitaxy and PSF/Wacker transistors had good electrical characteristics (Figures 4.12 a,d) and "soft" junction breakdown characteristics (Figures 4.12 b,c, f,g). The second set of PSF/Epitaxy transistors had lower gains than the second set PSF/Wacker transistors. However, the gains of the second set PSF/Wacker transistors were still significantly less than the gains of the first set PSF/Wacker transistors although both sets used the same materials and fabrication schedule. The second set of PSF/Epitaxy transistors exhibited saturation characteristics (Figure 4.12e) (at low base currents) which is possibly due to base punch though.

The recurring "soft" junction breakdown characteristics and decreasing transistor gains indicated a contaminated furnace. The quartz diffusion tubes and associated quartzware were etched to clean the furnaces (see Appendix D for procedure). Also all plastic and glass labware were cleaned (see Appendix D for procedure).

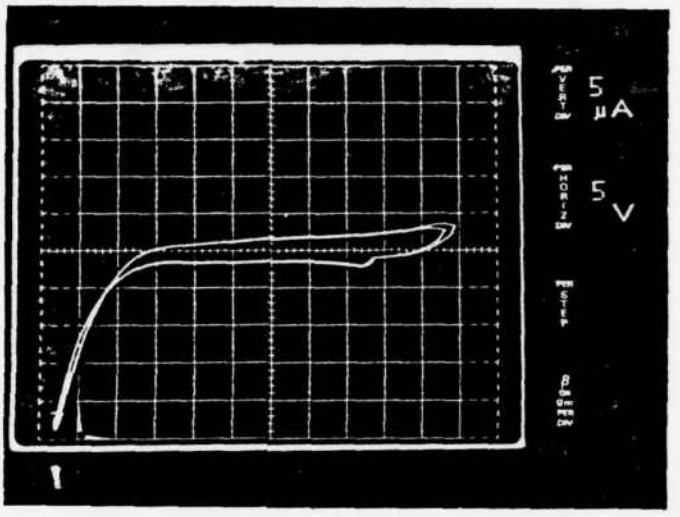


FIGURE 4.11a

Wacker Diode Reverse Bias Characteristics

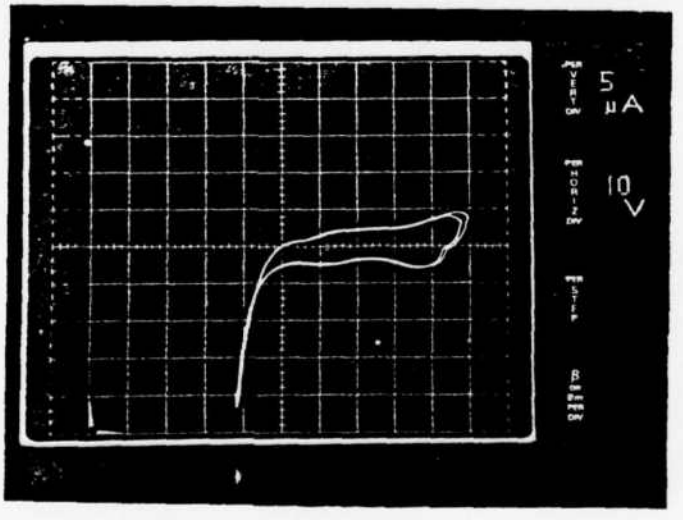


FIGURE 4.11b

Epitaxy Diode Reverse Bias Characteristics

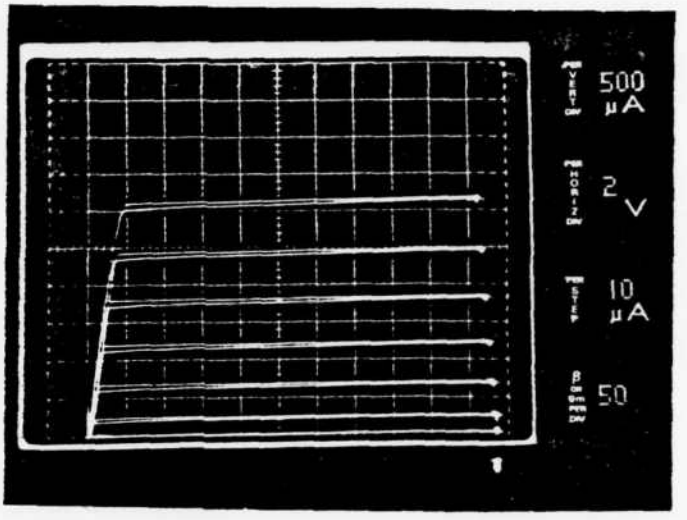
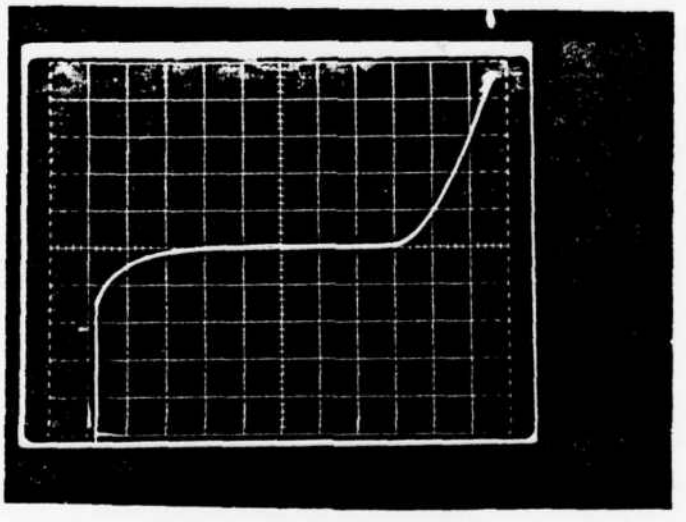


FIGURE 4.12a

Second Set PSF/Wacker Transistor I_c-V_{ce} Characteristics

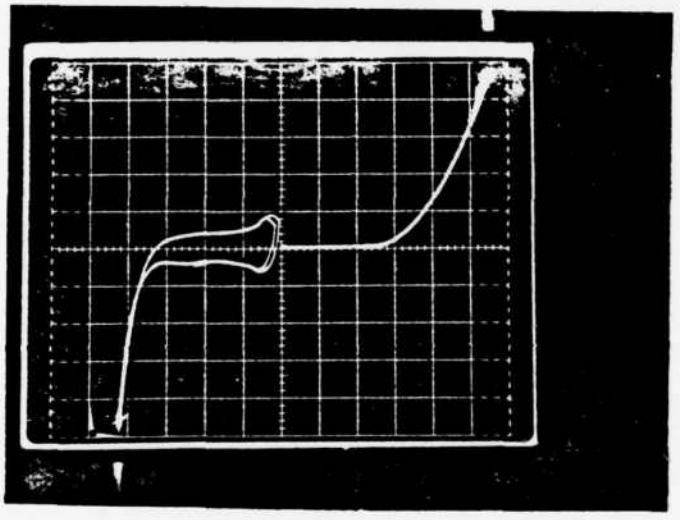


Forward Bias:
2 mA/div.
200 mV/div.

Reverse Bias:
10 μA/div.
2 V/div.

FIGURE 4.12b

Second Set PSF/Wacker Transistor Base-Emitter Junction Characteristics



Forward Bias:
1 mA/div.
200 mV/div.

Reverse Bias:
5 μA/div.
20 V/div.

FIGURE 4.12c

Second Set PSF/Wacker Transistor Base-Collector Junction Characteristics

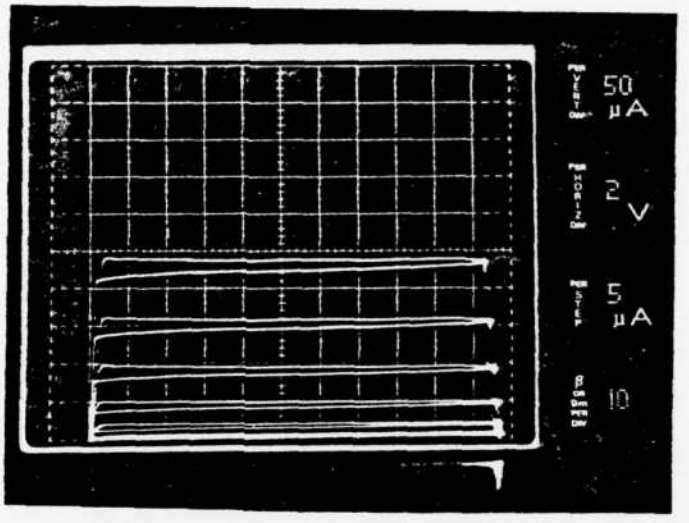


FIGURE 4.12d

Second Set PSF/Epitaxy Transistor I_c-V_{ce} Characteristics

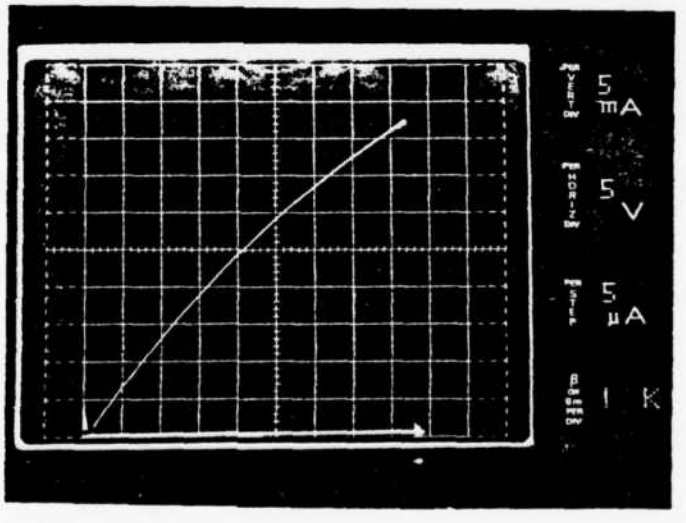
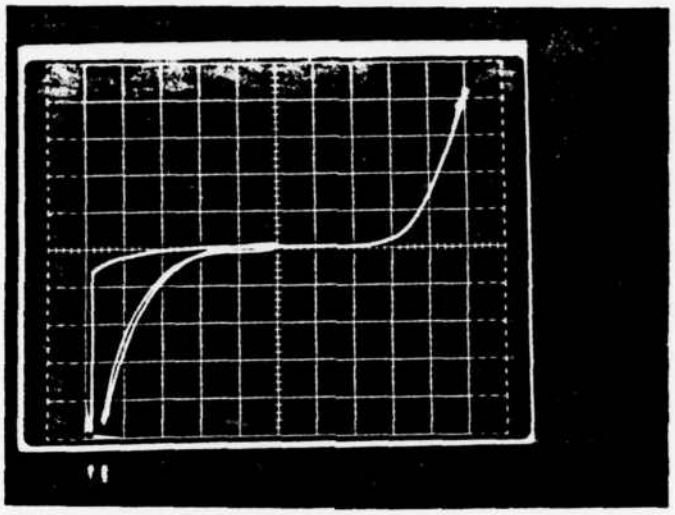


FIGURE 4.12e

Second Set PSF/Epitaxy Transistor

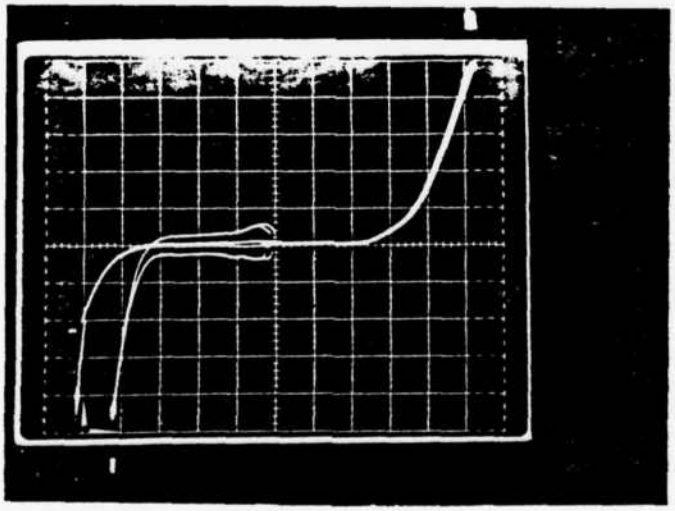


Forward Bias:
1 mA/div.
200 mV/div.

Reverse Bias:
5 μA/div.
lower trace
50 μA/div.
upper trace
2 V/div.

FIGURE 4.12f

Second Set PSF/Epitaxy Transistor Base-Emitter Junction Characteristics



Forward Bias:
500 μA/div.
200 mV/div.

Reverse Bias:
10 μA/div.
lower trace
100 μA/div.
upper trace
20 V/div.

FIGURE 4.12g

Second Set PSF/Epitaxy Transistor Base-Collector Junction Characteristics

Conventional transistors were again fabricated in Epitaxy and Wacker wafers using PSF for the emitter diffusion source (see Appendix C for fabrication schedule). Also a low concentration PSF source was mixed (one part PSF with $C_s = 5 \times 10^{20}$ phosphorus atoms per cm^3 and two parts silicafilm) and used as an emitter dopant source to observe emitter push at lower surface concentrations. The third set PSF/Epitaxy and PSF/Wacker transistors showed increases in gain (Figures 4.13 a,d; although Figure 4.13d shows a decrease in gain, on the average gain was increased), but the increases in gain of the third set transistors were still significantly lower than those of the first set of PSF/Wacker transistors. Paradoxically the junction characteristics of the third set PSF/Epitaxy and PSF/Wacker transistors (Figures 4.13 b,c,f,g) were not as good as those of the second set of PSF/Epitaxy and PSF/Wacker transistors indicating that the furnaces may not have been cleaned properly. An attempt to "tune up" the gain of PSF/Epitaxy transistors by increasing the emitter drive-in diffusion by a half hour did increase gains (Figure 4.13k) but the increased gains were still less than those of the first set PSF/Wacker transistors. The third set of PSF/Epitaxy transistors also showed saturation characteristics (Figure 4.13e), but the low concentration PSF/Epitaxy transistor did not exhibit such characteristics until after "tuning up" the transistor gains (Figure 4.13p) by increasing the emitter drive-in time by a half hour.

Gain and transistor breakdown voltages vs. transistor position on the wafer are plotted on Figures 4.14 a-e. There still existed wide variations in transistor gain and a variation in transistor breakdown voltage was also observed. Several transistors from the third set of PSF/Epitaxy and PSF/Wacker transistors were lapped and stained and the results (Table 4.5) were much more uniform than the gain measurements. The low concentration

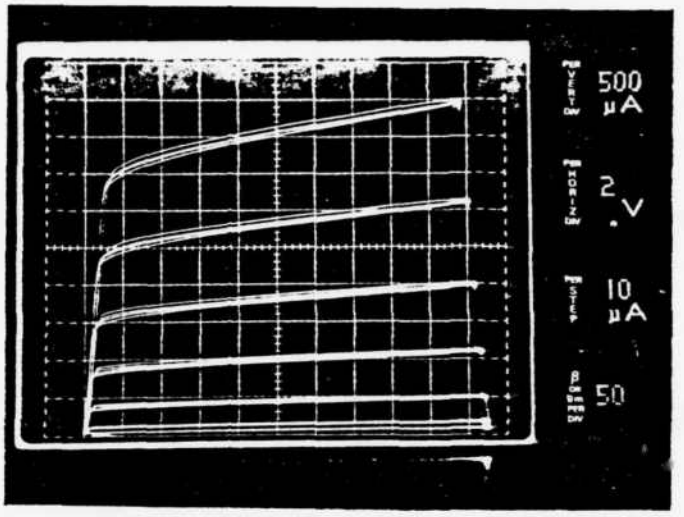
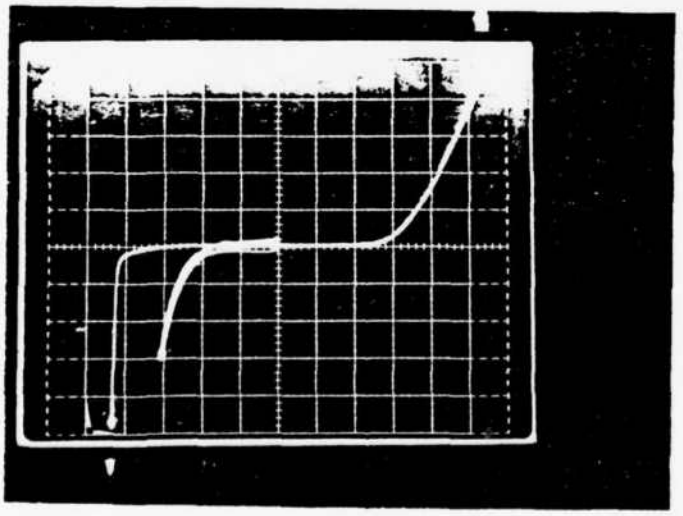


FIGURE 4.13a

Third Set PSF/Wacker Transistor I_c-V_{ce} Characteristics

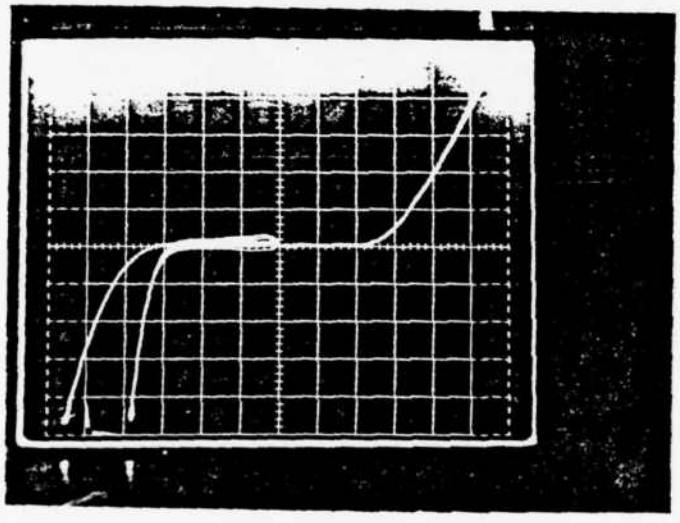


Forward Bias:
1 mA/div.
200 mV/div.

Reverse Bias:
5 μA/div.
lower trace
500 μA/div.
upper trace
2 V/div.

FIGURE 4.13b

Third Set PSF/Wacker Transistor Base-Emitter Junction Characteristics



Forward Bias:

500 μA/div.

200 mV/div.

Reverse Bias:

20 μA/div.
lower trace

200 μA/div.
upper trace

20 V/div.

FIGURE 4.13c

Third Set PSF/Wacker Transistor Base-Collector Junction Characteristics

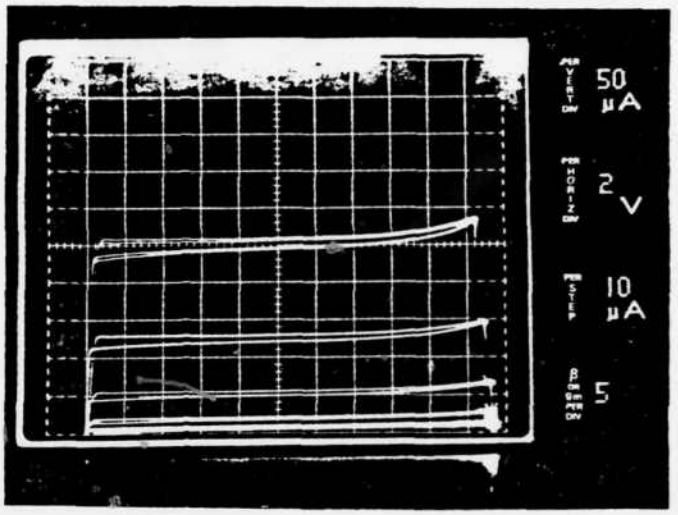


FIGURE 4.13d

Third Set PSF/Epitaxy Transistor I_c-V_{ce} Characteristics

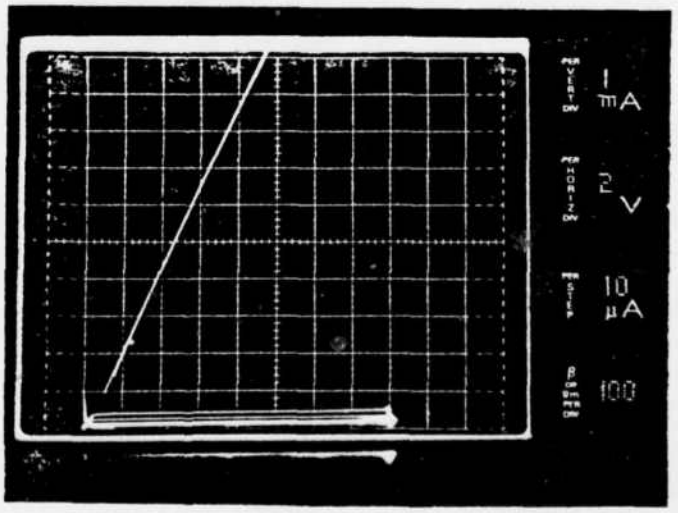
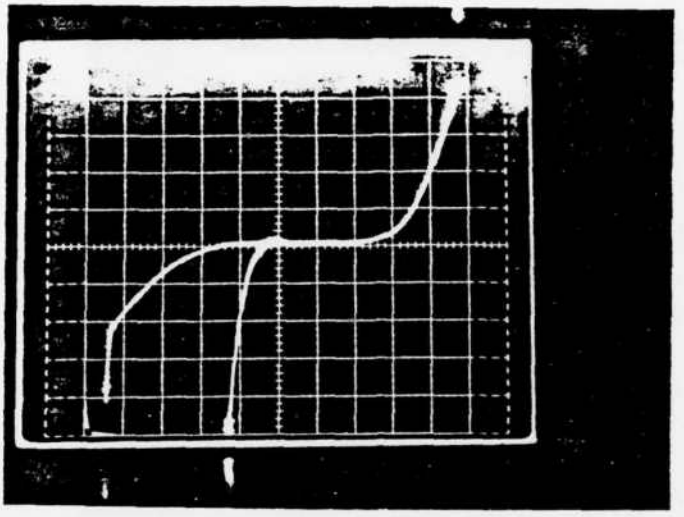


FIGURE 4.13e

Third Set PSF/Epitaxy Transistor

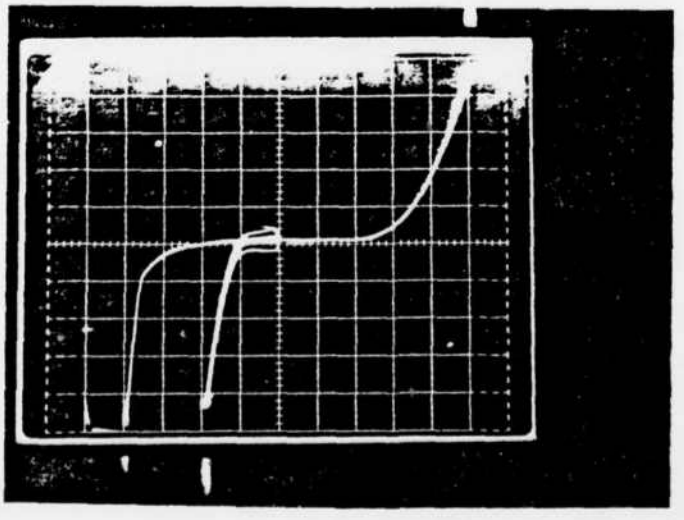


Forward Bias:
1 mA/div.
200 mV/div.

Reverse Bias:
10 μA/div.
lower trace
1 mA/div.
upper trace
2 V/div.

FIGURE 4.13f

Third Set PSF/Epitaxy Transistor Base-Emitter Junction Characteristics



Forward Bias:
500 μA/div.
200 V/div.

Reverse Bias:
10 μA/div.
lower trace
500 μA/div.
upper trace
20 V/div.

FIGURE 4.13g

Third Set PSF/Epitaxy Transistor Base-Collector Junction Characteristics

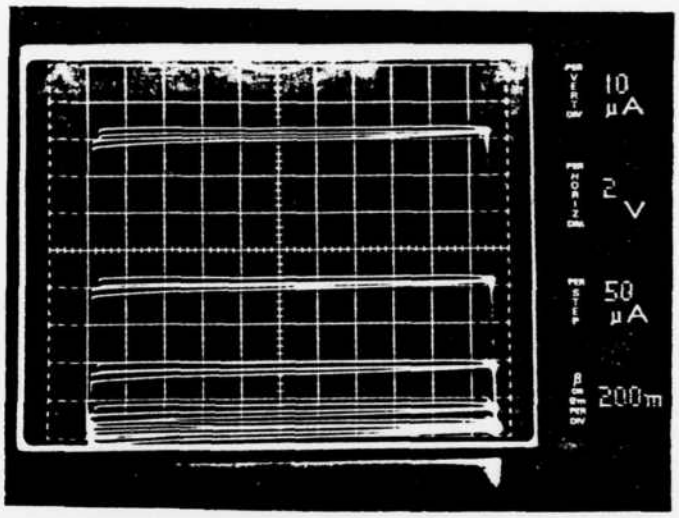
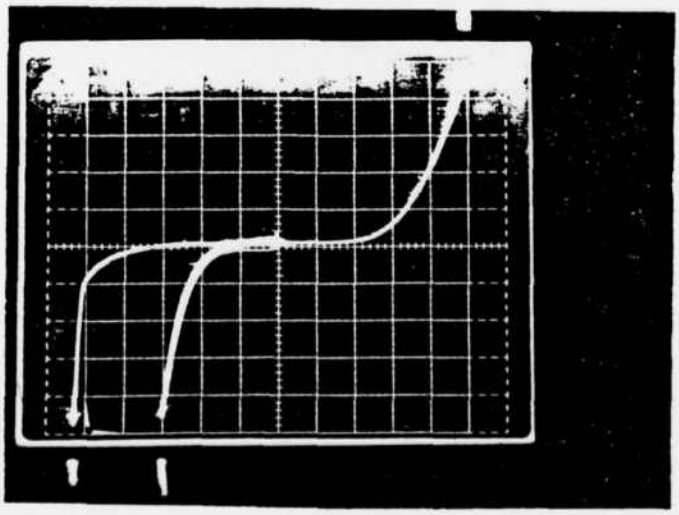


FIGURE 4.13h

Low Concentration PSF/Epitaxy Transistor I_c-V_{ce} Characteristics

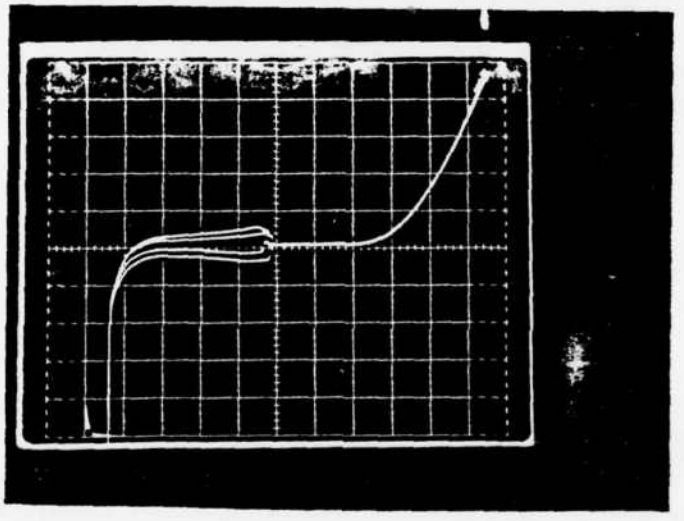


Forward Bias:
500 μA/div.
200 mV/div.

Reverse Bias:
5 μA/div.
lower trace
500 μA/div.
upper trace
2 V/div.

FIGURE 4.13i

Low Concentration PSF/Epitaxy Transistor
Base-Emitter Junction Characteristics



Forward Bias:
500 A/div.
200 mV/div.

Reverse Bias:
10 μA/div.
20 V/div.

FIGURE 4.13j

Low Concentration PSF/Epitaxy Transistor
Base-Collector Junction Characteristics

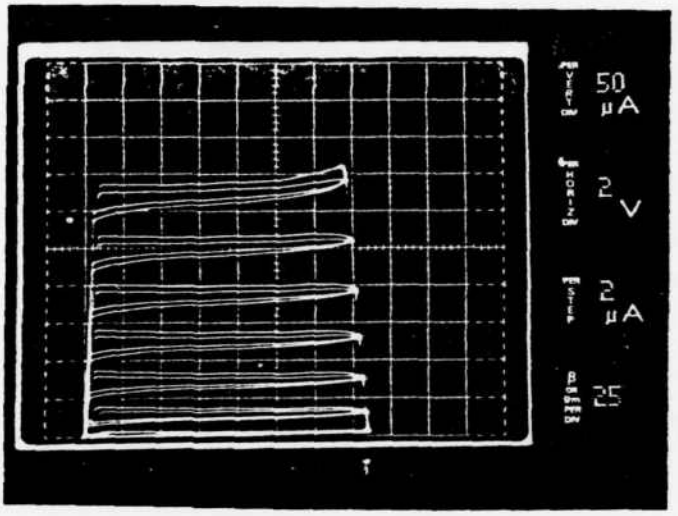


FIGURE 4.13k

PSF/Epitaxy, "tuned up" Transistor I_c-V_{ce} Characteristics

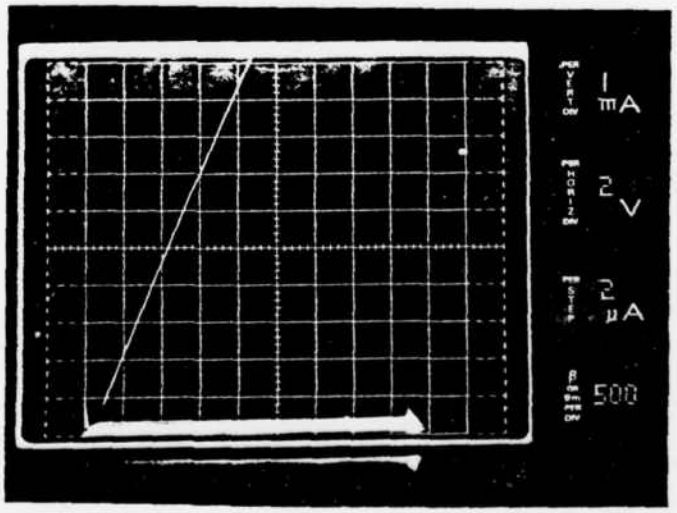
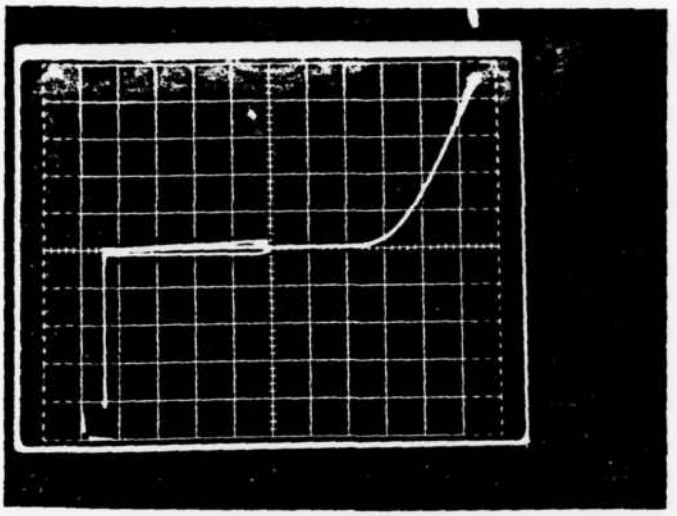


FIGURE 4.13l

PSF/Epitaxy, "tuned up" Transistor

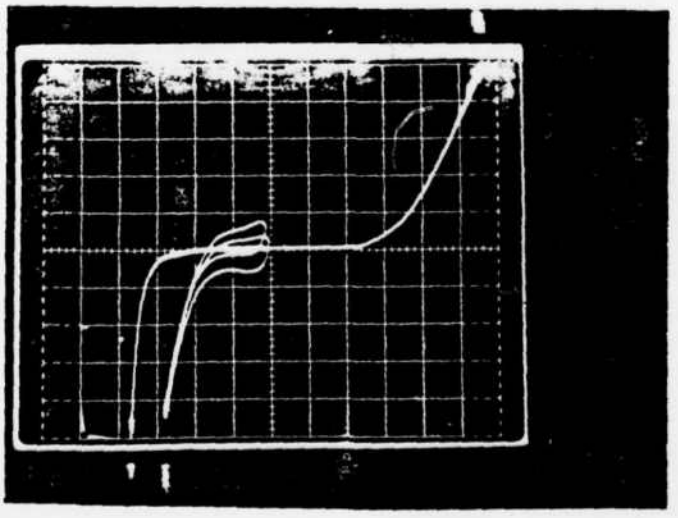


Forward Bias:
1 mA/div.
200 mV/div.

Reverse Bias:
5 μA/div.
2 V/div.

FIGURE 4.13m

PSF/Epitaxy, "tuned up" Transistor Base-Emitter Junction Characteristics



Forward Bias:
500 μA/div.
200 mV/div.

Reverse Bias:
5 μA/div.
lower trace
100 μA/div.
upper trace
20 V/div.

FIGURE 4.13n

PSF/Epitaxy, "tuned up" Transistor Base-Collector Junction Characteristics

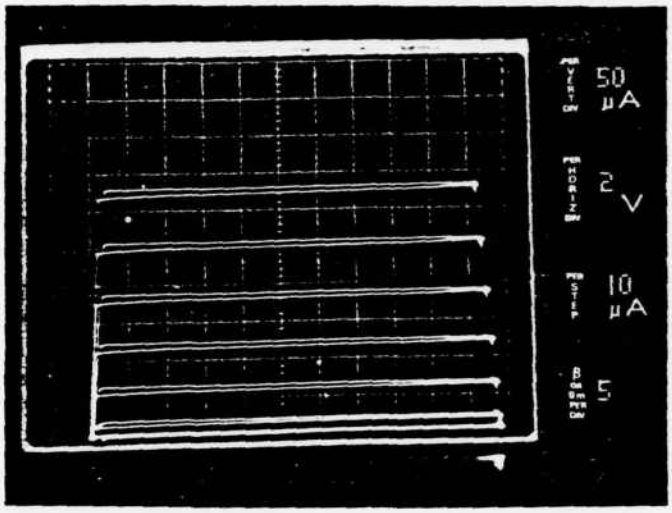


FIGURE 4.13o

Low Concentration PSF/Epitaxy, "tuned up" Transistor I_c-V_{ce} Characteristics

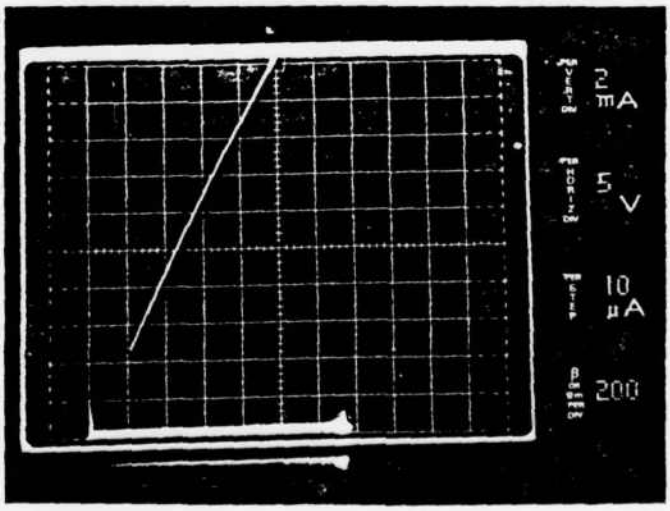
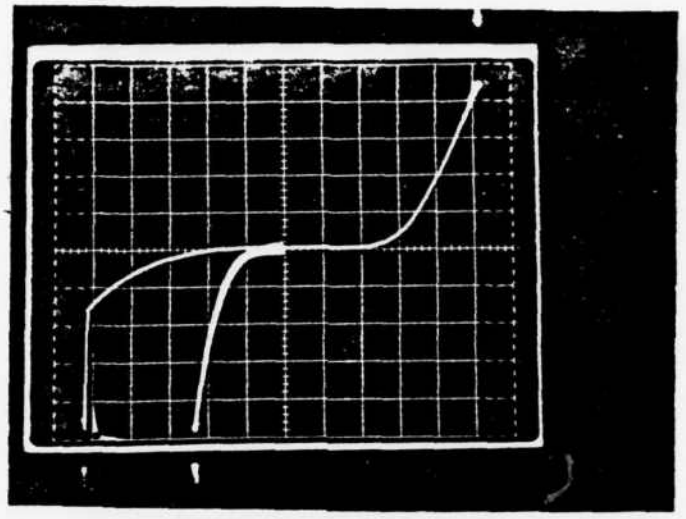


FIGURE 4.13p

Low Concentration PSF/Epitaxy, "tuned up" Transistor

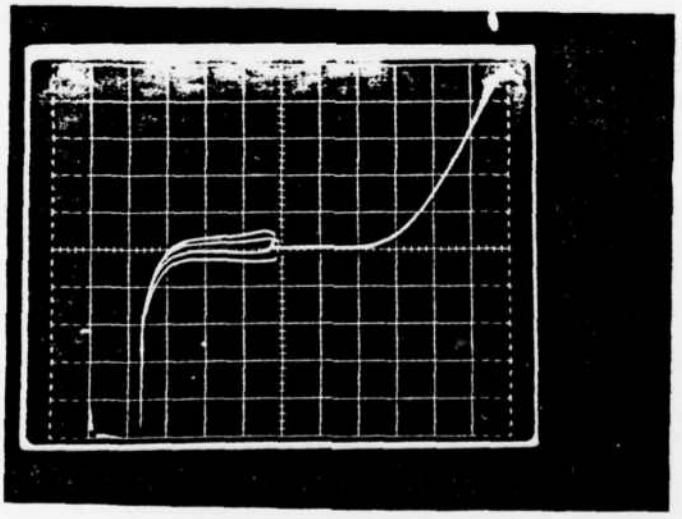


Forward Bias:
500 μA/div.
200 mV/div.

Reverse Bias:
5 μA/div.
lower trace
200 μA/div.
upper trace
2 V/div.

FIGURE 4.13q

Low Concentration PSF/Epitaxy, "tuned up" Transistor
Base-Emitter Junction Characteristics

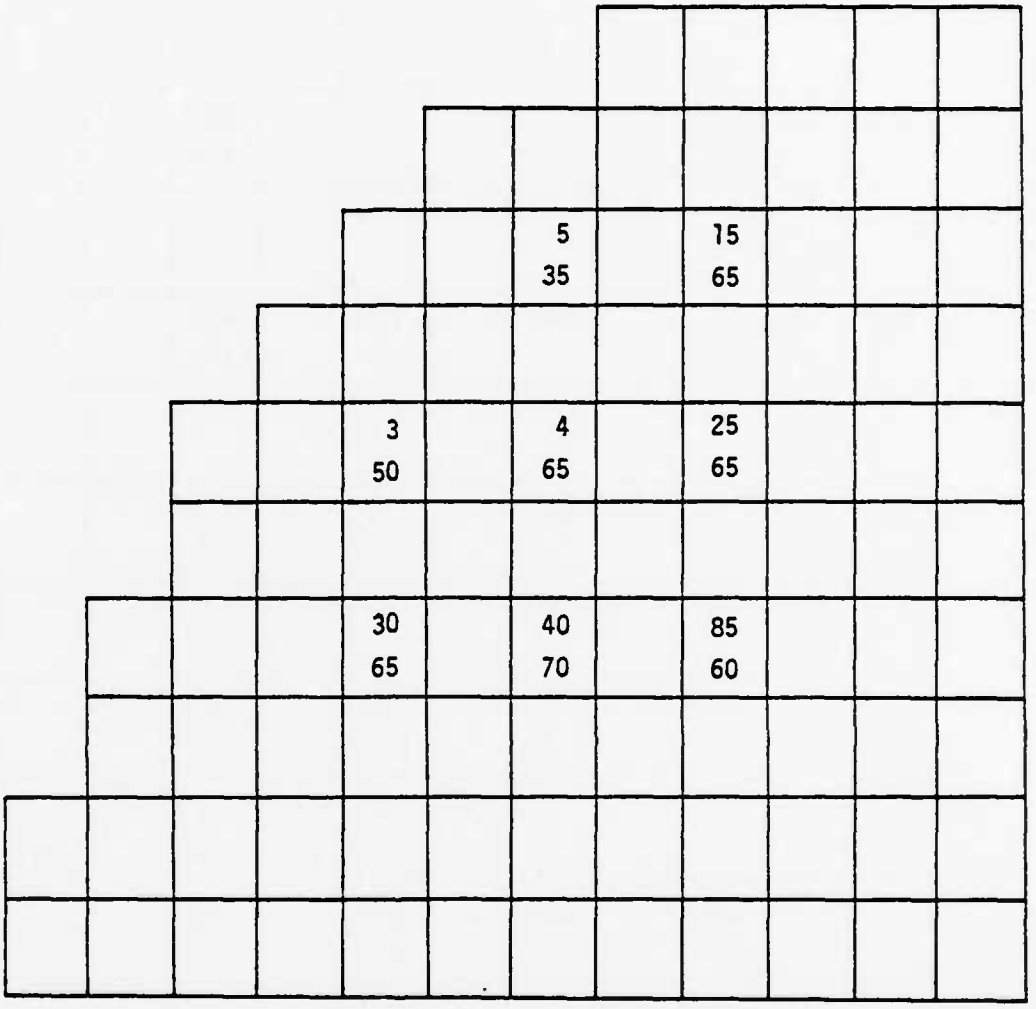


Forward Bias:
500 μA/div.
200 mV/div.

Reverse Bias:
10 μA/div.
20 V/div.

FIGURE 4.13r

Low Concentration PSF/Epitaxy, "tuned up" Transistor
Base-Collector Junction Characteristics



Base Current Step = 5 μA/step

Gain measurements taken between base steps #5 and #6 at 10V

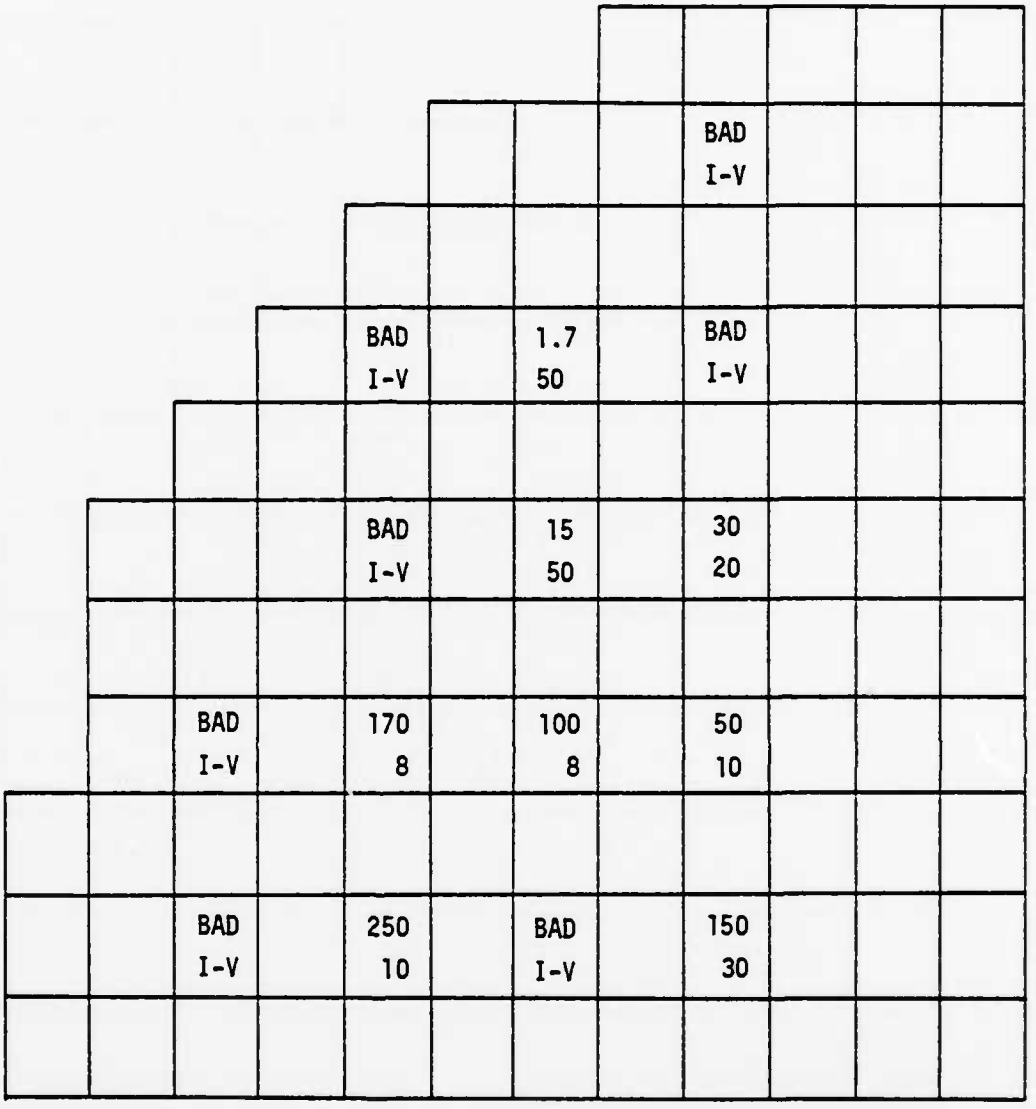
Each square corresponds to a transistor position

Top number = transistor gain

Bottom number = transistor breakdown voltage (volts)

FIGURE 4.14a

Third Set PSF/Wacker Transistor Gain and Breakdown Voltage vs. Position



Base current = 200 nA/step

Gain measurements taken between base steps #5 and #6 at 10V

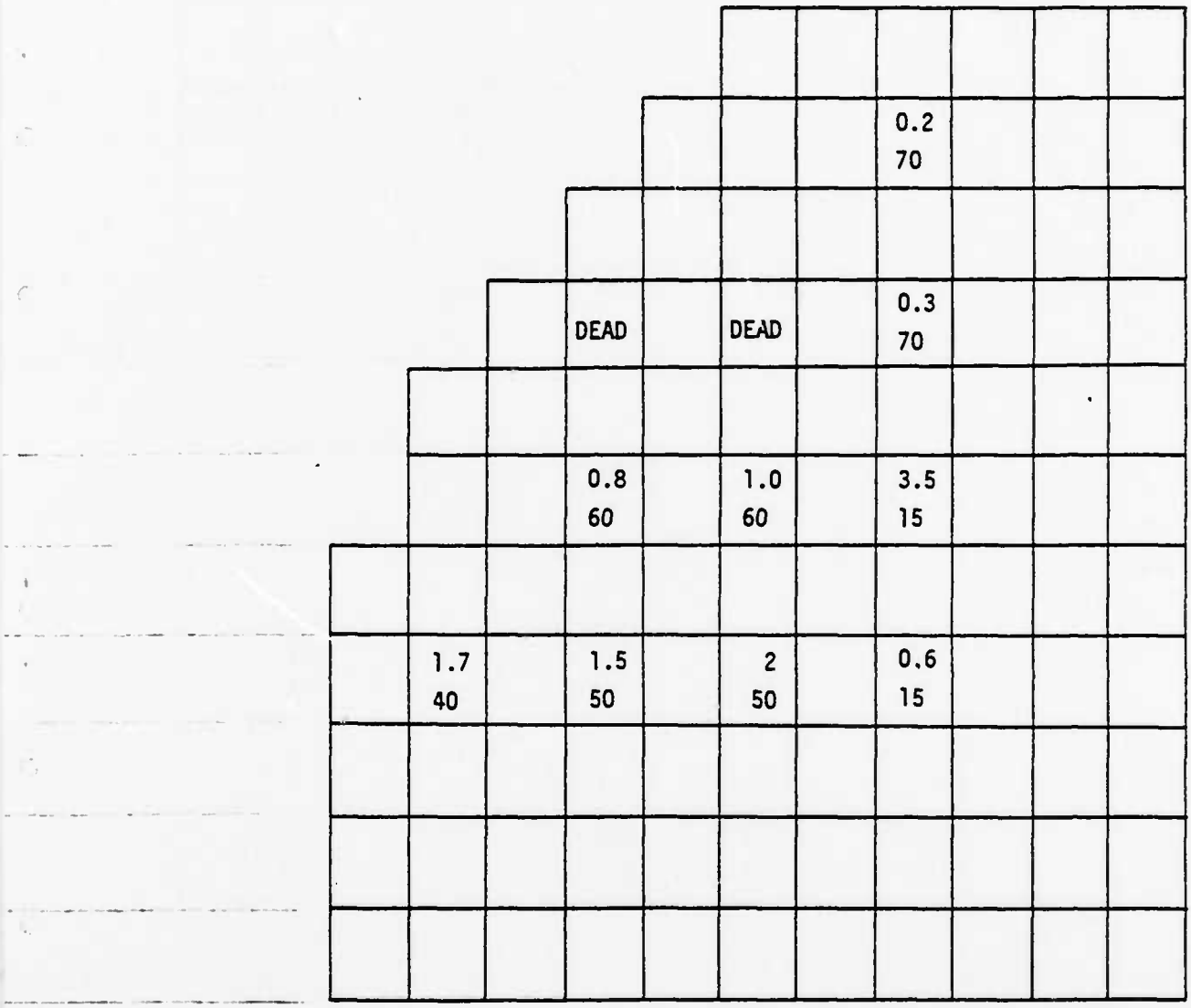
Each rectangle corresponds to a transistor position

Top number = transistor gain

Bottom number = transistor breakdown voltage (volts)

FIGURE 4 .14b

Third Set PSF/Epitaxy Transistor Gain and Breakdown Voltage vs. Position



Base Current = 100 μA/step

Gain measurements taken between base steps #5 and #6 at 10V

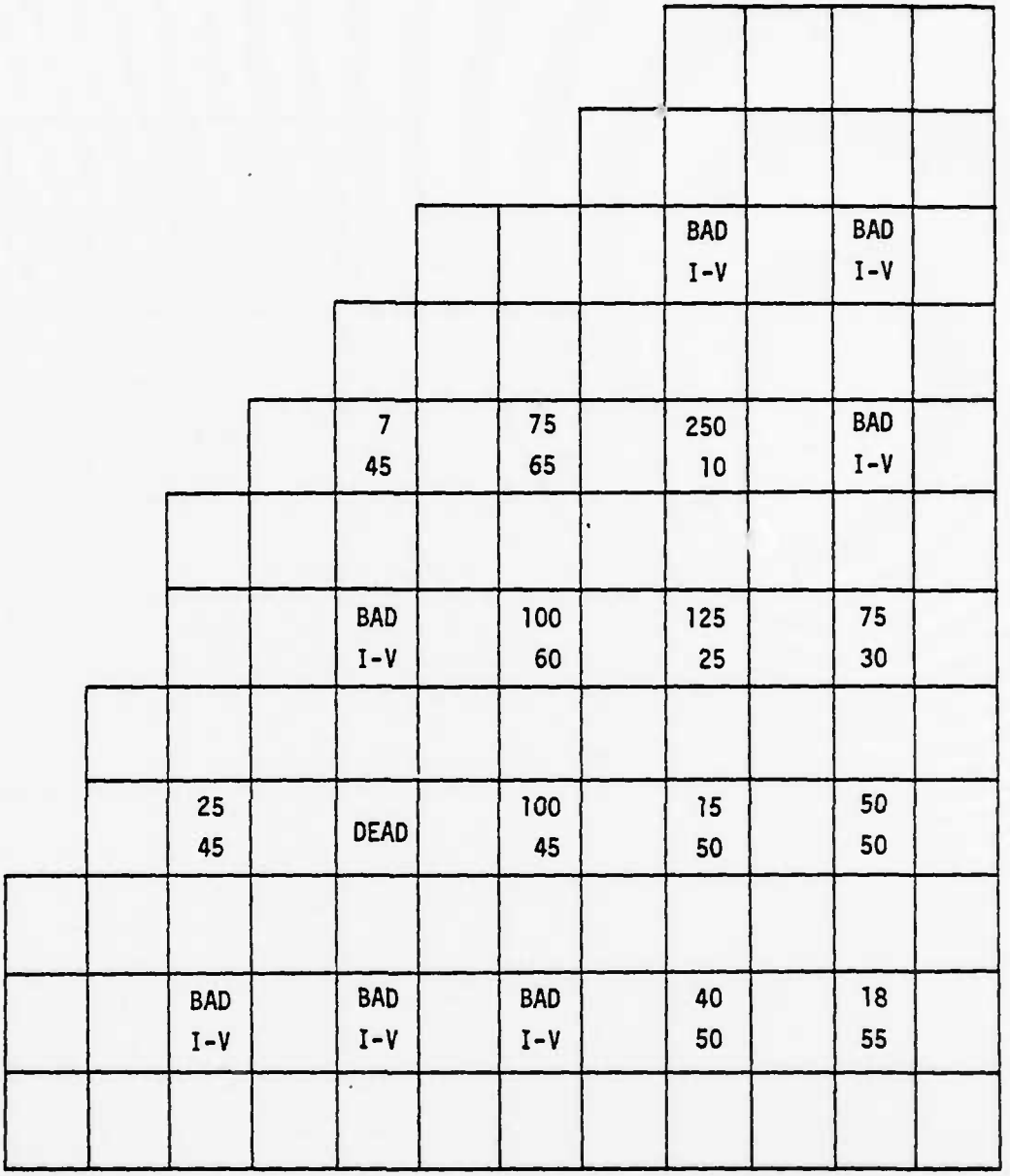
Each rectangle corresponds to a transistor position

Top number = transistor gain

Bottom number = transistor breakdown voltage (volts)

FIGURE 4.14c

Low Concentration PSF/Epitaxy Transistor
Gain and Breakdown Voltage vs. Position



Base current = 200 nA/step

Gain measurements taken between base steps #5 and #6 at 10V

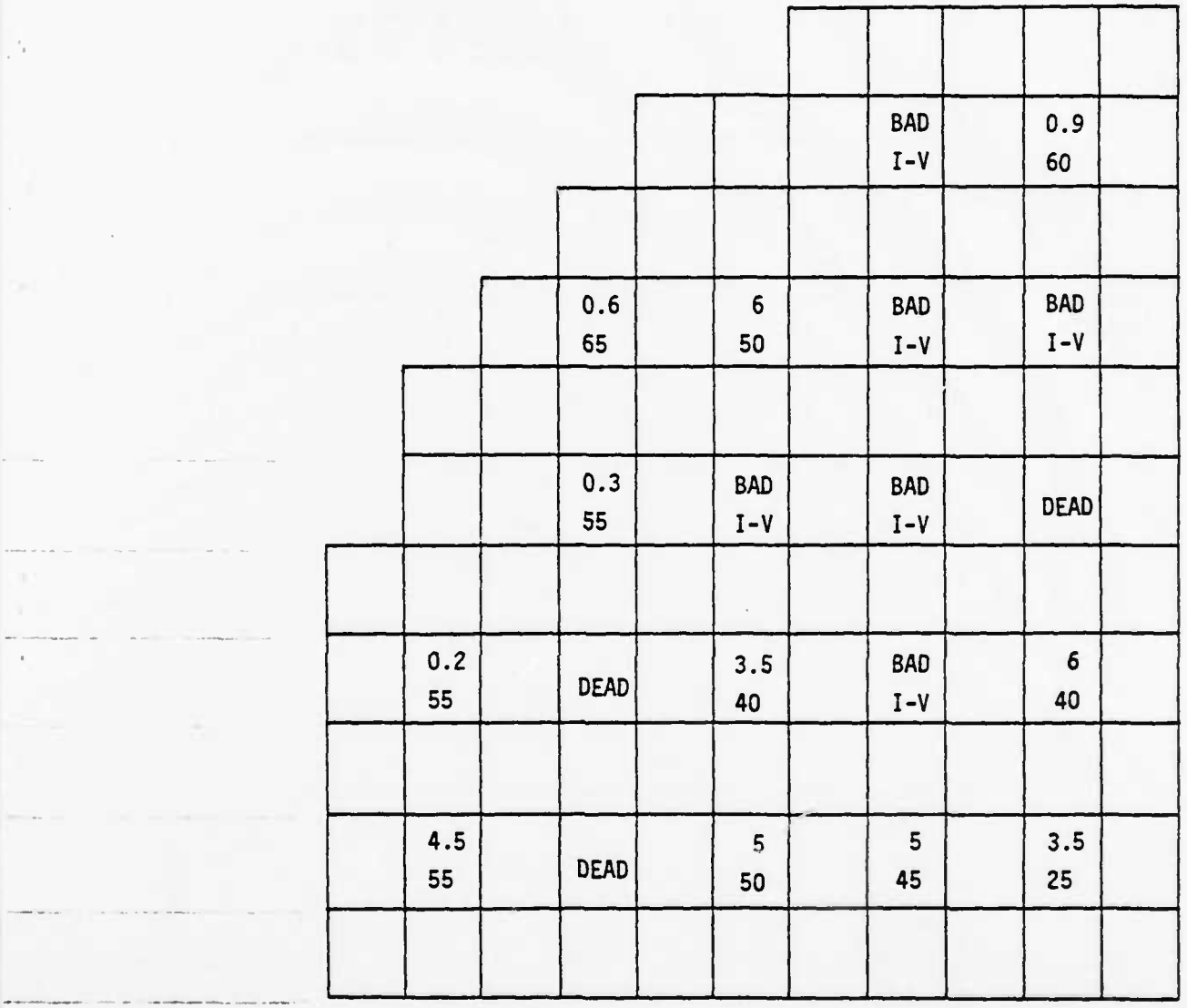
Each rectangle corresponds to a transistor position

Top number = transistor gain

Bottom number = transistor breakdown voltage (volts)

FIGURE 4.14d

PSF/Epitaxy, "tuned up" Transistor Gain and Breakdown Voltage vs. Position



Base current = 5 μA/step

Gain measurements taken between base steps #5 and #6 at 10V

Each rectangle corresponds to a transistor position

Top number = transistor gain

Bottom number = transistor breakdown voltage (volts)

FIGURE 4.14e

Low Concentration PSF/Epitaxy, "tuned up" Transistor Gain and Breakdown Voltage vs. Position

TABLE 4.5

Lap and Stain Measurements (μm)

Transistor Set	Emitter	Base	Push	Base Width	Epi Thickness
Third Set PSF/Wacker	2.5	3.0	0.5	1.0	
	2.1	3.0	0.7	1.6	
	2.7	*	*	-	
	2.5	2.8	0.5	0.8	
	2.7	*	*	-	
	2.3	2.5	0.3	0.5	
Third Set PSF/Epitaxy	*	3.3	0.3	-	10.6
	2.0	3.4	0.3	1.7	10.6
	2.1	3.3	0.3	1.5	11.0
	*	3.3	0.5	-	11.0
	2.7	3.8	0.3	1.4	12.2
	*	3.8	0.7	-	12.2

*bad junction delineation

AD-A132 331 EFFECTS OF SIMULTANEOUS PHOSPHORUS AND ARSENIC DIFFUSIONS ON EMITTER PUSH..(U) HAWAII UNIV AT MANOA HONOLULU DEPT OF ELECTRICAL ENGINEERING..

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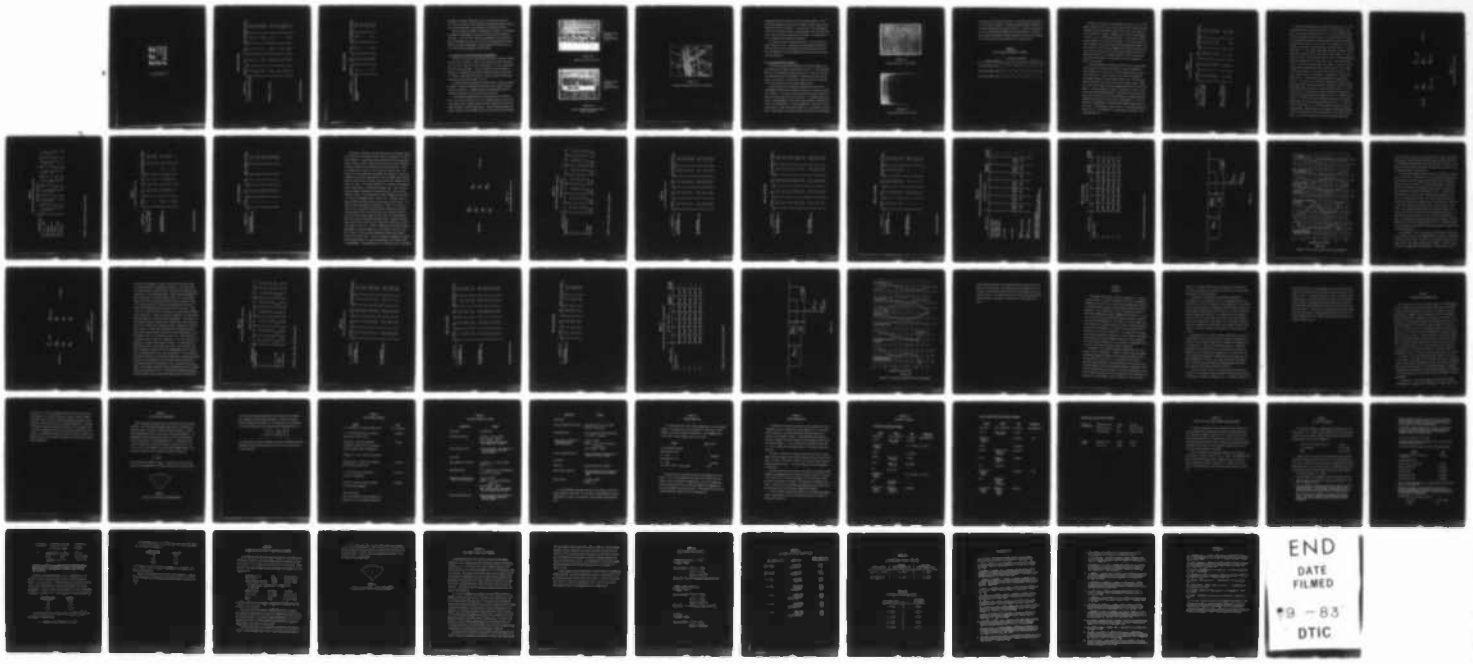

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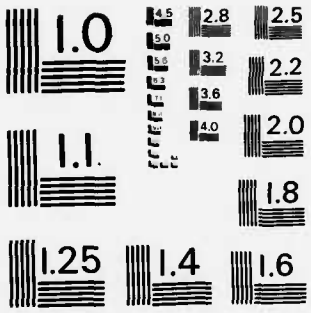

MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS - 1963 - A

TABLE 4.5 (continued)

Transistor Set	Emitter	Base	Push	Base Width	Epi Thickness
Low Concentration PSF/Epitaxy	1.2	3.3	0	2.1	11.9
	1.2	3.3	0	2.1	11.9
	0.7	3.2	0	2.5	10.6
	0.7	*	0	-	10.6
	1.0	3.0	0	2.0	10.6
	1.0	3.3	0	2.3	10.6
PSF/Epitaxy, "tuned up"	2.5	3.4	0.2	1.1	9.9
	2.8	3.6	0.3	1.1	10.2
	*	3.3	*	-	9.3
	2.8	3.3	*	-	9.3
	*	3.2	0.1	-	10.3
	1.9	3.3	*	-	10.3
	2.0	3.2	0.2	1.4	9.9
	1.7	3.3	0.2	1.8	9.9

*bad junction delineation

TABLE 4.5 (continued)

Transistor Set	Emitter	Base	Push	Base Width	Epi Thickness
Low Concentration PSF/Epitaxy, "tuned up"	1.1	3.6	0.1	2.6	11.8
	1.1	3.6	0.1	2.6	11.9
	*	3.5	*	-	10.6
	*	3.8	*	-	11.9
	*	3.3	*	-	11.9
	1.3	3.6	0.1	2.4	11.9
	*	3.4	0.1	-	11.9

*bad junction delineation

PSF/Epitaxy transistors exhibited little or no emitter push, possibly due to the lower dopant surface concentration approaching borderline emitter push concentrations and/or the shallowness of the emitter diffusions.

After reviewing the attempts to improve gain uniformity, it was decided to abandon gain measurements to monitor the effects of the simultaneous diffusions. It was felt that significant improvements in gain uniformity was not forthcoming and work with lap and stain techniques and dislocation etchants had shown these methods to produce uniform results that are sensitive to possible simultaneous diffusion effects.

4.3 Lap and Stain and Dislocation Density Measurements

The work on lap and stain techniques paralleled the attempts to improve transistor gain uniformity. Several staining solutions were tested including 1-3-10, 50-5, and 50-6 Cu stains (see Appendix E for stain compositions and lap and stain procedure). The 1-3-10 solution junction delineation appeared to be produced by the solution etching n-type and p-type material at different rates instead of staining. The 50-6 Cu solution produced the best junction delineation (Figures 4.15 a,b).

A scanning electron microscope was used to observe a cleaved transistor structure. Although the cleaved surface could be seen, junction delineation was not possible. A specimen current collecting probe may have revealed the junctions, but such a probe was not available.

The dislocation etchants tests also paralleled the gain uniformity work. The Sirtl etch (works well on (111) surfaces) was the first dislocation etchant tested. Numerous dislocations were revealed by the Sirtl etch around the edges of heated treated wafers. These dislocations formed slip planes (Figure 4.16) that extended from the front to the back of the wafers.

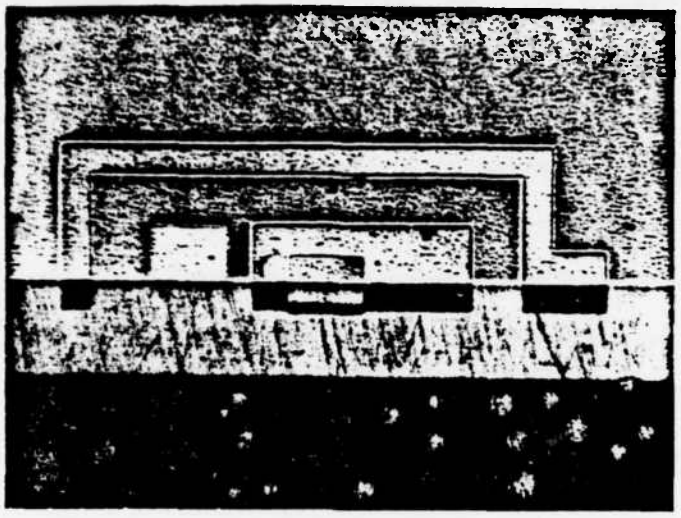

FIGURE 4.15a

Lapped and Stained Transistor

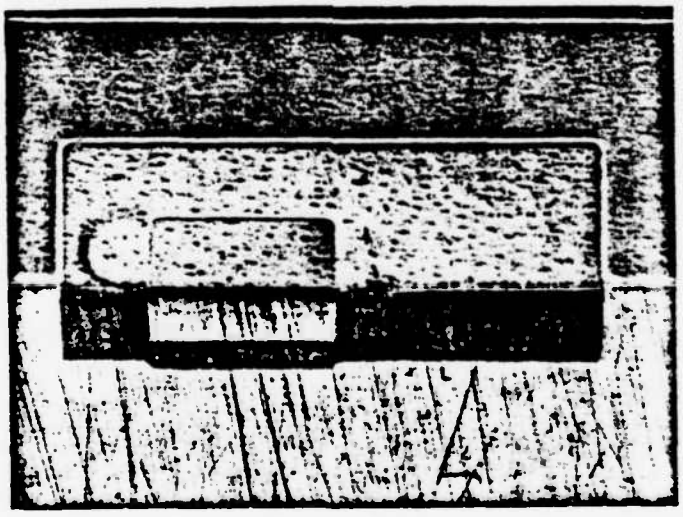

FIGURE 4.15b

Lapped and Stained Transistor Section
(Base and Emitter)

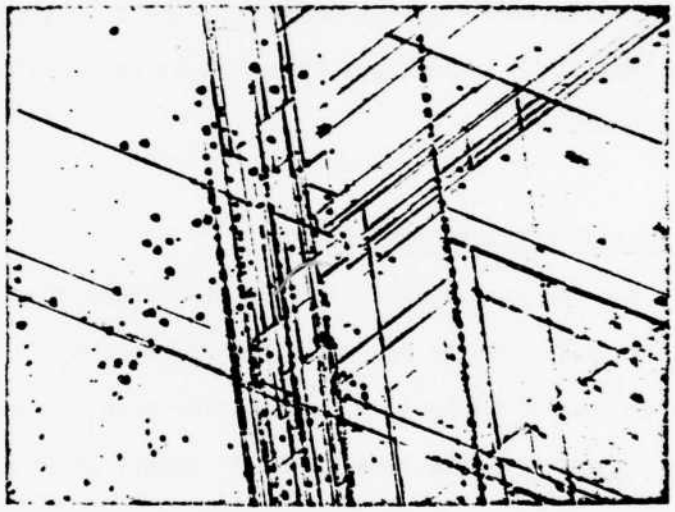

FIGURE 4.16

Thermally Induced Slip Planes in (111) Wafer

Unprocessed wafers did not exhibit such dislocation formation. These dislocations appeared to be the result of thermal stresses caused by rapid heating and cooling of the wafers. A slow push/pull rate (approximately three to four inches per minute) to introduce wafers into the furnace tube and to remove the wafers eliminated the slip planes. The elimination of the slip planes did not improve gain uniformity.

The Wright etch was also tested (works well on (111) and (100) surfaces) (Figures 4.17 a,b). The Wright etch produced better defined dislocation etch pits and less extraneous surface texturing from the Sirtl etch (see Appendix F for etchant compositions and etching and dislocation counting procedures).

4.4 Dual Dopant Emitter Transistors

Since the low concentration PSF/Epitaxy transistors produced little or no emitter push, higher concentration PSF with $C_s = 1 \times 10^{21}$ phosphorus atoms per cm^3 was obtained to ensure emitter push. A special mix ASF was also obtained that had the same number of dopant atoms per gram SiO_2 and same SiO_2 concentration in the spin-on solution as the high concentration PSF to facilitate the mixing of the dual dopant sources.

The base diffusions for transistor structures to be used for the simultaneous diffusions were fabricated as identically as possible to maintain uniformity. Four Epitaxy wafers were quartered (sixteen quarters) to serve as the wafer material for the transistors. The Epitaxy wafers were chosen to take advantage of the epitaxial layer thickness in monitoring the lap and stain measurements. The boron predeposition, using boron nitride planar sources, of the sixteen wafer quarters plus a test wafer per lot was done in three batches (n-type Wacker material were used as the test wafers).

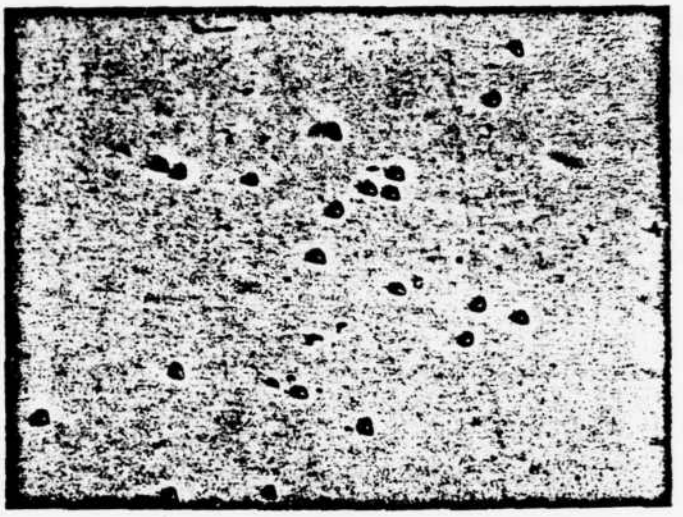

FIGURE 4.17a

Wright Etched (111) Silicon Wafer

FIGURE 4.17b

Wright Etched (100) Silicon Wafer

The base drive-in diffusions were done all at the same time (see Appendix C fo. base diffusion schedule). However, the measured sheet resistances of the three batches were not the same (Table 4.6). The sheet resistances of the first and second base predeposition diffusion batches (six quarters each) were 80 and 82 ohms per square, respectively, and the third predeposition diffusion batch (four quarters) was 71 ohms per square.

TABLE 4.6

Sheet Resistance Measurements (Ω/square)

Diffusion Source	position on the wafer 1	2	3	4	5	$\overline{\rho_s}$	$\overline{x}$
First Base Predep. Batch	81	81	80	80	81	81	0.6
Second Base Predep. Batch	82	82	81	81	83	82	0.8
Third Base Predep. Batch	70	69	71	72	71	71	1.1

Conventional transistors were fabricated using ASF with $C_s = 2 \times 10^{20}$ arsenic atoms per cm^3 for the emitter diffusion source in wafers from base predeposition diffusion batches two and three to check the uniformity of the base diffusions. Table 4.7 summarizes the lap and stain measurements of the ASF, $C_s = 2 \times 10^{20}$/Epitaxy transistors. A small amount of emitter push was observed from the ASF diffused emitter. The junction depths are almost identical for the second and third base predeposition batches. However, the gain of the third base predeposition diffusion ASF-Epitaxy transistors were less than those of the second base predeposition diffusion ASF/Epitaxy transistors. An attempt was made to use the third base predeposition diffusion wafers with periphery mixes of the phosphorus to arsenic ratio spectrum.

A constant phosphorus concentration was maintained in the dual dopant spin-on sources and the arsenic concentration varied to determine the optimum phosphorus to arsenic ratio in the dual dopant source at the diffusing conditions to minimize emitter push and dislocation generation. The constant phosphorus concentration was chosen at 8.2×10^{21} phosphorus atoms per gram SiO_2 to facilitate mixing the dual dopant sources. Appendix G lists the dual dopant source mix compositions and outlines the mixing method. A minor discrepancy was noted for the special mix arsenic spin-on source upon comparing the manufacturer's published arsenic atoms per gram SiO_2 and our calculated ratio from the manufacturer's published weight percentages at the special mix arsenic spin-on (see Appendix G). It was assumed that the manufacturer's published arsenic atoms per gram SiO_2 ratio was correct. The phosphorus to arsenic ratio in the dual dopant source was chosen from 1:1 to 5:1 phosphorus to arsenic based on the results of the M. Watanabe study [3].

TABLE 4.7

Lap and Stain Measurements (μm)

Transistor Set	Emitter	Base	Push	Base Width	Epi Thickness
ASF, $C_s = 2 \times 10^{20}$/Epitaxy,	0.4	3.6	0.2	3.4	12.3
Second Base Predep. Batch	0.4	3.6	0.2	3.4	12.3
	0.4	3.6	0.1	3.3	12.2
	0.4	3.6	0.1	3.3	12.2
	0.2	3.8	0.1	3.7	13.0
	0.5	3.8	0.1	3.4	13.0
ASF, $C_s = 2 \times 10^{20}$/Epitaxy,	*	3.6	0.1	-	11.7
Third Base Predep. Batch	0.3	3.6	*	-	11.5
	0.3	3.6	0.1	3.4	12.1
	0.3	3.6	0.1	3.4	11.9

*bad junction delineation

Conventional transistors were fabricated using ASF with $C_s = 4 \times 10^{20}$ arsenic atoms per cm^3, dilute PSF which had 8.2×10^{21} phosphorus atoms per gram SiO_2, and dilute ASF which had 8.2×10^{21} arsenic atoms per gram SiO_2 for the emitter diffusion sources. P-type Wacker wafers were doped with the aforementioned emitter diffusion sources in addition to the high concentration PSF, special mix ASF, and a 3:1 dual dopant source to measure the sheet resistance of the diffused layers from these sources. The lighter doped wafer (i.e., lower dopant concentration sources) and slower diffusing species were placed "up wind" in the diffusion furnace tube (i.e., closer to the end of the diffusion tube with the gas inlet) to minimize outgassing effects (arrangement shown in Figure 4.18). All of the test wafers were slightly cloudy after the spun-on glass was removed. The special mix ASF diffused layer surface had brown particle swirls and the 3:1 dual dopant diffused layer surface was very cloudy with brown particle swirls. The water cleaning procedure (see Appendix B) succeeded only in removing the particle swirls. The sheet resistance measurements are summarized in Table 4.8. The special mix ASF and high concentration PSF sources exhibited higher sheet resistances than their counterpart lower dopant concentration dilute ASF and dilute PSF. Several of the ASF with $C_s = 4 \times 10^{20}$, dilute ASF and dilute PSF emitter diffused transistors were lapped and stained and the measurements are tabulated in Table 4.9. Although the ASF with $C_s = 4 \times 10^{20}$ and dilute ASF transistors had higher arsenic surface concentrations than the previously fabricated ASF with $C_s = 2 \times 10^{20}$ transistors, the ASF with $C_s = 4 \times 10^{20}$ and dilute ASF transistors exhibited no emitter push. Repeated efforts to delineate the arsenic doped emitters failed which indicated that possibly the arsenic did not diffuse into the wafer. The dilute PSF transistors exhibited significant emitter push.

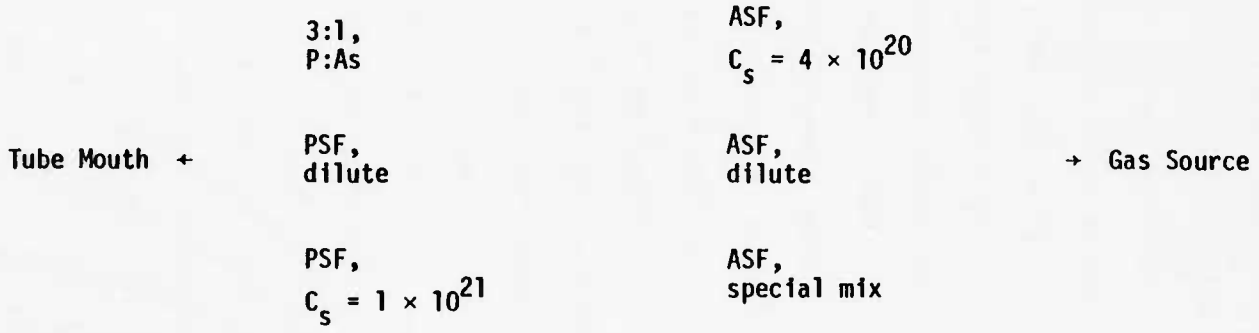

FIGURE 4.18

Wafer Arrangement During Diffusions

TABLE 4.8

Sheet Resistance Measurements (Ω/square)

Diffusion Source	position on the wafer 1	2	3	4	5	$\overline{\rho_s}$	$\bar{x}$
ASF, $C_s = 4 \times 10^{20}$	1607	1236	1246	872*	1482	1390	180
ASF, dilute	604	451	548	372	370	469	104
ASF, special mix	2295	2074	2189	1404*	1926	2121	160
PSF, dilute	7.8	9.1	8.2	8.5	8.9	8.5	0.5
PSF, $C_s = 1 \times 10^{21}$	23	31	33	53*	35	31	5
3:1, P:As mix	11.0	13.6	10.6	10.0	11.5	11.3	1.4

*omitted in average sheet resistance calculations

TABLE 4.9

Lap and Stain Measurements (μm)

Transistor Set	Emitter	Base	Push	Base Width	Epi Thickness
ASF, $C_s = 4 \times 10^{20}$/Epitaxy, First Base Predep. Batch	*	4.0	0	-	11.6
	*	4.0	0	-	11.6
	*	3.7	0	-	11.9
	*	3.8	0	-	11.9
PSF, dilute/Epitaxy, Second Base Predep. Batch	2.6	3.8	*	-	11.7
	2.5	3.6	0.5	1.6	11.7
	*	3.6	0.3	-	11.9
	*	3.6	0.3	-	11.8
	2.5	3.7	0.4	1.6	*
	2.7	*	*	-	*

*bad junction delineation

TABLE 4.9 (continued)

Transistor Set	Emitter	Base	Push	Base Width	Epi Thickness
ASF, dilute/Epitaxy Second Base Predep. Batch	*	3.6	0	-	12.1
	*	3.6	0	-	11.7
	*	3.3	0	-	11.8
	*	3.3	0	-	11.5
	*	3.6	0	-	12.3
	*	3.6	0	-	12.1
	*	3.6	0	-	11.7
	*	3.6	0	-	12.0
	*	3.6	0	-	12.3
	*	3.6	0	-	12.1

*bad junction delineation

Conventional transistors were fabricated using the dual dopant sources and dilute ASF for the emitter diffusion sources (see Appendix C for fabrication schedule). P-type Wacker wafers were doped with the aforementioned emitter diffusion sources in addition to the dilute PSF source to measure the sheet resistance of the diffused layers from these sources. Prior to the predeposition diffusion, all of the spun-on films were clear. The spun-on films were cloudy after the predeposition diffusion, increasing in cloudiness as the arsenic concentration in the dual dopant glass increased. After the spun-on glass was removed, some residual swirls remained and the surface was cloudy. The surface cloudiness also increased with increasing arsenic concentration in the removed dual dopant glass. Again, the wafer cleaning procedure (see Appendix B) removed the swirls, but the surface cloudiness remained. An error was made in wafer placement during the emitter diffusions (arrangement shown in Figure 4.19). The wafers with the higher concentration emitter diffusion sources were placed "up wind". The sheet resistance measurements are summarized in Table 4.10. There was an increase in the dilute PSF diffused layer sheet resistance from the previous measurement (Table 4.8) which made the sheet resistance from the dilute PSF diffused layers higher than those from the high concentration PSF diffused layers (a much more consistent result). Several of the dual dopant and dilute ASF transistors were lapped and stained and the results are tabulated in Table 4.11. Table 4.12 summarizes the dislocation density measurements of test wafer doped with the dual dopant sources and dilute ASF in addition to the boron base predeposition diffusions, dilute PSF source, and the N-250 source. Figure 4.20 graphically summarizes the sheet resistance measurements, lap and stain measurements, and dislocation density measurements. Although emitter push is minimized at the 3:1 dual dopant

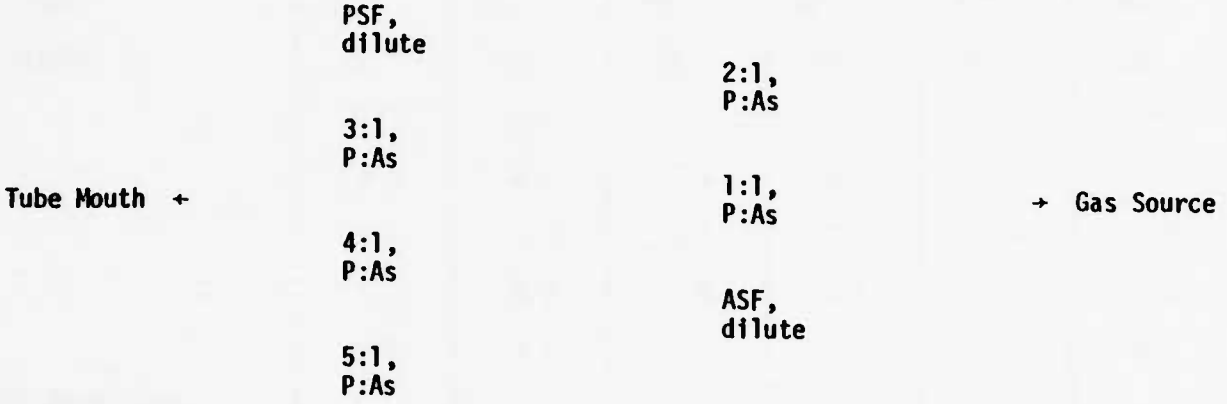

FIGURE 4.19

Wafer Arrangement During Diffusions

TABLE 4.10

Sheet Resistance Measurements (Ω/square)

Diffusion Source	position on the wafer 1	2	3	4	5	$\overline{\rho_s}'$	$\bar{x}$
Phosphorus:Arsenic							
1:1	4.8	4.7	5.1	5.8	5.3	5.1	0.4
2:1	5.1	5.0	5.8	6.1	6.8	5.8	0.7
3:1	7.3	7.0	8.0	8.9	7.6	7.8	0.7
4:1	5.5	5.1	6.1	5.6	6.4	5.7	0.5
5:1	5.9	5.6	6.5	6.2	7.0	6.2	0.5
PSF, dilute	58	58	58	59	57	58	0.7
ASF, dilute	1141	1075	1002	957	325*	1040	80

*omitted in average sheet resistance calculations

TABLE 4.11

Lap and Stain Measurements (μm)

Transistor Set	Emitter	Base	Push	Base Width	Epi Thickness
1:1, P:As/Epitaxy, Second Base Predep. Batch	3.3	3.6	0.7	1.0	11.9
	3.4	3.6	0.7	0.9	12.0
	3.3	3.6	0.7	1.0	11.9
	3.3	3.7	0.7	1.1	11.9
	3.3	3.6	0.6	0.9	12.3
	3.2	3.6	0.6	1.0	12.2
2:1, P:As/Epitaxy, Second Base Predep. Batch	3.1	3.6	0.6	1.1	11.7
	3.1	3.7	0.6	1.2	11.5
	3.2	3.8	0.7	1.3	11.9
	3.2	3.7	0.3	0.8	11.8
	3.0	3.6	0.6	1.2	11.6
	3.0	3.6	0.7	1.3	11.4

TABLE 4.11 (continued)

Transistor Set	Emitter	Base	Push	Base Width	Epi Thickness
3:1, P:As/Epitaxy, Third Base Predep. Batch	2.8	3.6	0.5	1.3	12.2
	2.8	3.7	0.5	1.4	12.3
	2.8	3.6	0.5	1.3	11.4
	2.7	3.5	0.5	1.3	11.4
	2.6	3.5	0.5	1.4	11.9
	2.6	3.5	0.4	1.3	12.1
	2.7	3.4	0.5	1.2	10.7
	2.6	3.4	0.5	1.3	10.8
	2.7	3.5	0.5	1.3	11.1
	2.7	3.4	0.5	1.2	11.2
4:1, P:As/Epitaxy, First Base Predep. Batch	3.3	3.6	0.7	1.0	12.6
	3.3	3.7	0.7	1.1	12.6
	3.1	3.3	0.6	0.8	12.0
	3.1	3.3	0.5	0.7	11.8
	3.2	3.5	0.6	0.9	12.1
	3.1	3.5	0.6	1.0	11.9

TABLE 4.11 (continued)

Transistor Set	Emitter	Base	Push	Base Width	Epi Thickness
5:1, P:As/Epitaxy, Second Base Predep. Batch	3.0	3.5	0.5	1.0	11.7
	3.0	3.5	0.5	1.0	11.6
	3.2	3.5	0.5	0.8	11.7
	3.1	3.6	0.5	1.0	11.6
	3.1	3.4	0.6	0.9	11.7
	3.0	3.5	0.5	1.0	11.5
ASF, dilute/Epitaxy, First Base Predep. Batch	*	3.6	0	-	11.9
	*	3.6	0	-	11.9
	*	3.6	0	-	11.1
	*	3.6	0	-	11.3
	*	3.7	0	-	11.9
	*	3.7	0	-	11.7

*bad junction delineation

TABLE 4.12a

Dislocation Density Measurements (dislocations/cm^2)

Diffusion Source	position on the wafer 1	2	3	4	5	Average Density	$\bar{x}$	# Times Etched
Boron Base Diffusions:								
First Predep. Batch	-	-	-	-	-			2
Second Predep. Batch	-	-	-	-	-			1
Third Predep. Batch	-	-	-	-	-			1
PSF, dilute	-	-	-	-	-			3
	-	-	-	-	-			3
ASF, dilute	29,400	47,100	17,700*	41,200	-**	39,200	9,000	1
	35,300	41,200	17,700*	35,300	-**	37,300	3,400	2
N-250, used n-type (111) wafer	2,600	700*	1,300	2,900	1,900	2,200	700	1
N-250, used p-type (100) wafer	-	-	-	-	-			1

-less than 500 dislocations/cm^2
*omitted in average dislocation density calculations
**extraneous surface texturing made measurements impossible

TABLE 4.12b (continued)

Diffusion Source	position on the wafer 1	2	3	4	5	Average Density	$\bar{x}$	# Times Etched
Phosphorus:Arsenic								
1:1	70,700	64,200	44,200*	60,700	73,000	67,200	5,700	1
2:1	18,300	5,900*	13,000*	26,000	29,400	24,600	5,700	2
3:1	26,500	25,900	5,900*	33,000	44,200	32,400	8,500	1
4:1	33,600	18,800	8,800*	30,600	27,700	27,700	6,400	1
5:1	53,000	59,000	26,500*	38,300	50,100	50,100	8,700	1

*omitted in average dislocation density calculations

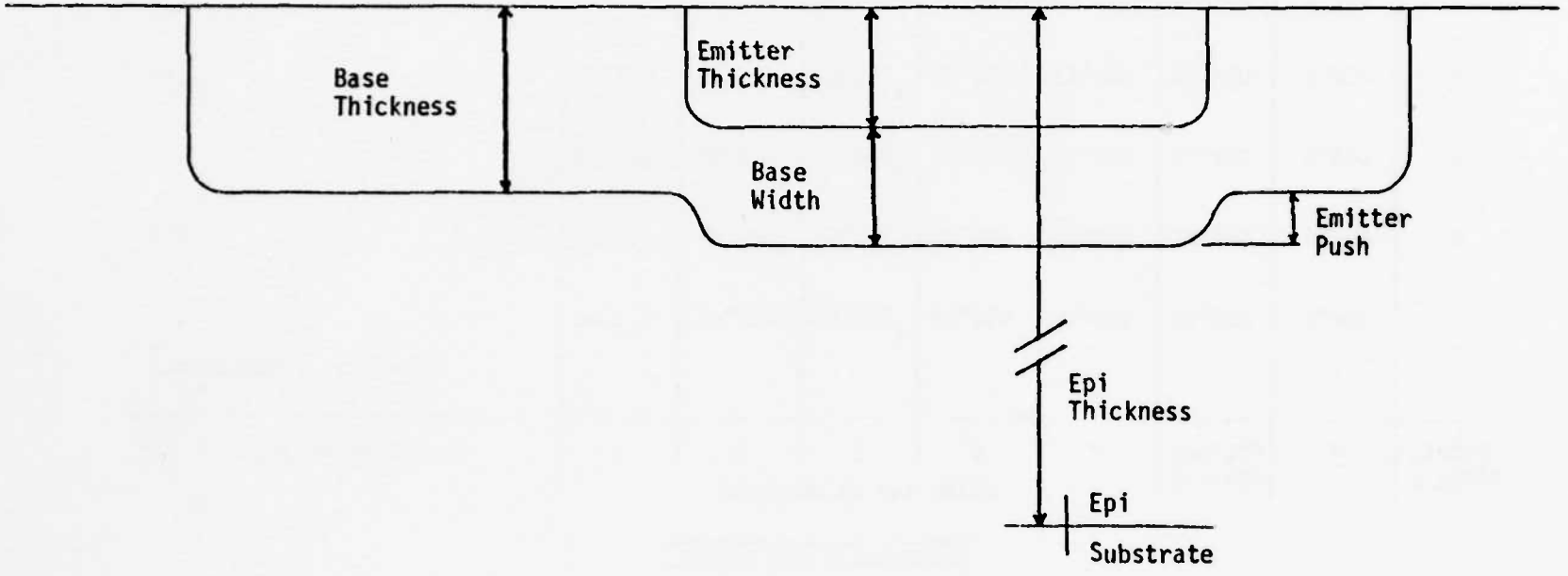
Base
Thickness
Emitter
Thickness
Base
Width
Emitter
Push
Epi
Thickness
Epi
Substrate

FIGURE 4.20a

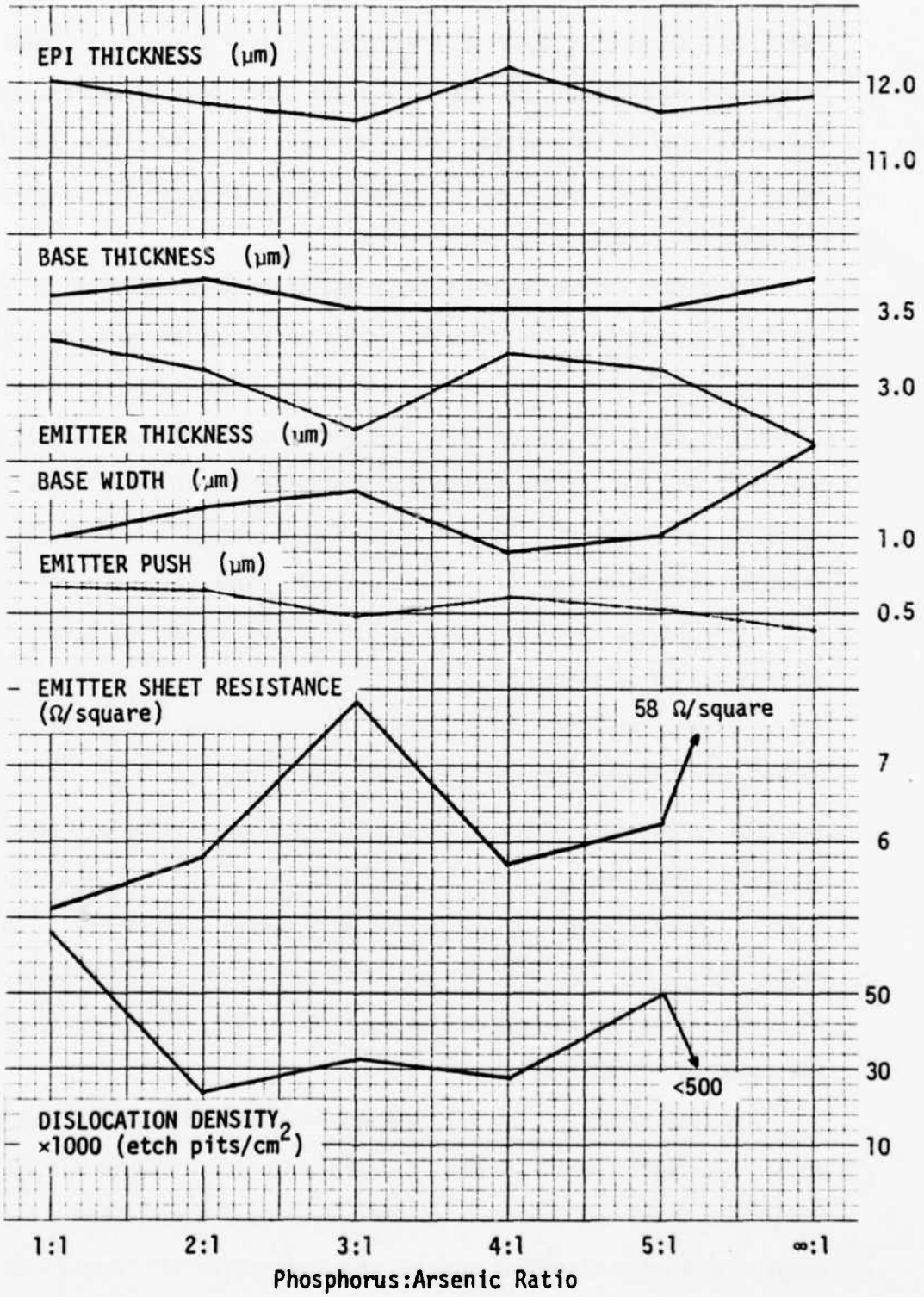

FIGURE 4.20b

Summary of the First Dual Dopant Transistor Measurements

ratio, the sheet resistance of the diffused layer from the 3:1 dual dopant source was much higher than those from the other dual dopant sources and the corresponding base-emitter junction much shallower. Thus the 3:1 dual dopant transistors exhibited the widest base region, which may have caused our observed reduction in emitter push.

The Wright etch produced surface texturing that appeared to delineate swirls or striation. The observed swirls or striation were concentric defect patterns on the wafer surface and the surface texturing diminished toward the center of the wafers. The boron base diffusion, dilute PSF, and N-250 on (100) wafers all produced diffused layers with surface dislocation densities less than 500 dislocations per cm^2. The minimum dislocation density of the dual dopant diffused layers occurred at the 2:1 and 4:1 dual dopant source ratios. The 2:1 dual dopant diffused layer surface had to be etched twice before etch pits were observed. There was a significant decrease in dislocation density toward the center of the wafers. The dilute ASF diffused layer surface exhibited extensive surface texturing after etching, making etch pit observation difficult. Unprocessed and processed (one hour in O_2 at 1100^oC and a subsequent one hour in N_2) Epitaxy and p-type Wacker wafers were also etched. The p-type Wacker wafers had less than 500 dislocations per cm^2. The Epitaxy wafers exhibited extensive surface texturing after etching making dislocation etch pit counting impossible.

The shallowness of the 3:1 dual dopant diffused layer was attributed to an incorrectly mixed 3:1 dual dopant source and a second 3:1 dual dopant source was mixed and used in a second set of dual dopant transistors (the other ratios of dual dopant sources were not remixed). Figure 4.21 shows the wafers arrangement during the diffusions. There were little or no

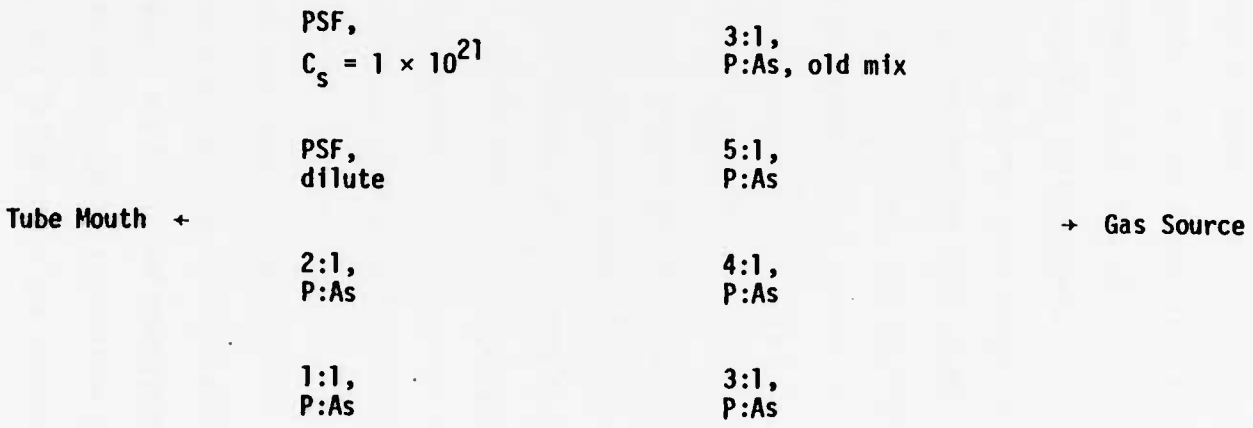

FIGURE 4.21

Wafer Arrangement During Diffusions

particle swirls remaining on the wafer surface after the spun-on glass was removed following the predeposition diffusion. The surface cloudiness trend reversed; increasing surface cloudiness with decreasing arsenic concentration in the dual dopant source. Sheet resistance measurements of the diffused layers from the dual dopant sources, old 3:1 dual dopant source, dilute and high concentration PSF sources are tabulated in Table 4.13. The diffused layers from the high concentration PSF source had higher sheet resistances than those from the dilute PSF source. Tables 4.14 and 4.15 summarizes the lap and stain and dislocation density measurements, respectively. Figure 4.22 graphically summarizes the lap and stain, sheet resistance, and dislocation density measurements. The second set of dual dopant transistors produced emitter diffused layer sheet resistances that uniformly decreased with decreasing arsenic concentration in the dual dopant sources. A trend toward increased emitter diffused layer depth from the dual dopant sources with decreasing arsenic concentration in the dual dopant sources is also observed in Figure 4.22. This observation is in agreement with the report by M. Watanabe et.al. that the diffusivity of phosphorus is reduced by the presence of arsenic. A slight reduction in emitter push at the 2:1 dual dopant source ratio is also observed. However, the amount of reduction is within the measurement limits of the lap and stain techniques used in our study (see Appendix E for error margins). The dilute PSF transistors exhibited the lowest amount of emitter push which may be due to the shallowness of the dilute PSF emitter diffused layer. The dislocation density was minimized at the 3:1 dual dopant source ratio. However, the dislocation densities that were measured was very high (greater than 25,000 dislocations per cm^2). The dilute PSF diffused layer surface dislocation density was less than 500 dislocations per cm^2 (equivalent to

TABLE 4.13

Sheet Resistance Measurements (Ω/square)

Diffusion Source	position on the wafer 1	2	3	4	5	$\overline{\rho_s}$	$\bar{x}$
Phosphorus:Arsenic							
1:1	6.1	6.0	7.3	6.0	8.0	6.7	0.9
2:1	6.3	6.4	5.8	6.0	6.4	6.2	0.3
3:1	5.0	5.0	5.5	5.8	6.1	5.5	0.5
4:1	4.9	4.8	5.4	5.4	5.5	5.2	0.3
5:1	4.6	4.6	5.0	5.1	5.2	4.9	0.3
PSF, $C_s = 1 \times 10^{21}$	155	174	143	98*	161	158	13
PSF, dilute	11.8	10.0	11.2	8.1*	16.2	12.3	2.7
3:1, old P:As mix	9.4	14.4*	10.0	10.1	9.2	9.7	0.4

*omitted in average sheet resistance calculations

TABLE 4.14

Lap and Stain Measurements (μm)

Transistor Set	Emitter	Base	Push	Base Width	Epi Thickness
1:1, P:As/Epitaxy, Third Base Predep. Batch	3.0	3.6	0.6	1.2	11.5
	3.0	3.6	0.6	1.2	11.3
	3.0	3.5	0.6	1.1	10.3
	2.9	3.6	0.5	1.2	9.9
	3.1	3.6	0.6	1.1	11.1
	3.0	3.6	0.6	1.2	10.8
	3.1	3.6	0.6	1.1	11.6
	3.1	3.6	0.7	1.2	11.3
2:1, P:As/Epitaxy, First Base Predep. Batch	2.9	3.4	0.5	1.0	12.3
	2.9	3.4	0.5	1.0	11.9
	3.0	3.6	0.6	1.2	11.9
	3.0	3.6	0.5	1.1	11.9
	3.0	3.6	0.5	1.1	12.4
	3.0	3.6	0.6	1.2	12.3

TABLE 4.14 (continued)

Transistor Set	Emitter	Base	Push	Base Width	Epi Thickness
3:1, P:As/Epitaxy, First Base Predep. Batch	*	3.8	0.7	-	11.9
	3.3	3.6	0.6	0.9	12.0
	3.2	3.6	0.6	1.0	11.8
	3.0	3.6	0.6	1.2	11.6
	3.3	3.5	0.7	0.9	12.3
	3.3	3.5	0.7	0.9	11.9
4:1, P:As/Epitaxy, First Base Predep. Batch	3.4	3.7	0.6	0.9	12.3
	3.4	3.6	0.7	0.9	11.9
	2.8	3.3	0.5	1.0	10.5
	2.9	3.2	0.5	0.8	10.3
	3.2	3.3	0.6	0.7	11.5
	3.0	3.4	0.7	1.1	11.1
	3.3	3.4	0.6	0.7	11.8
	3.3	3.4	0.6	0.7	11.6

*bad junction delineation

TABLE 4.14 (continued)

Transistor Set	Emitter	Base	Push	Base Width	Epi Thickness
5:1, P:As/Epitaxy, Third Base Predep. Batch	3.3	3.8	0.7	1.2	11.3
	3.1	3.8	0.6	1.3	11.1
	3.2	3.6	0.6	1.0	10.9
	3.2	3.6	0.5	0.9	10.8
	3.3	3.8	0.7	1.2	11.6
	3.4	3.6	0.7	0.9	11.5

TABLE 4.15

Dislocation Density Measurements (dislocations/cm^2)

Diffusion Source	position on the wafer 1	2	3	4	5	Average Density	$\bar{x}$	# Times Etched
Phosphorus:Arsenic								
1:1	66,000	66,000	63,600	67,100	61,800	64,900	2,100	2
2:1	47,100	33,000	34,700	53,600	52,400	44,200	9,700	2
3:1	28,900	24,700	20,000	23,000	23,600	24,000	3,200	2
4:1	40,600	37,700	32,400	46,500	43,600	40,200	5,500	2
5:1	30,600	36,500	11,800*	24,700	32,400	31,100	4,900	2

*omitted in average dislocation density calculations

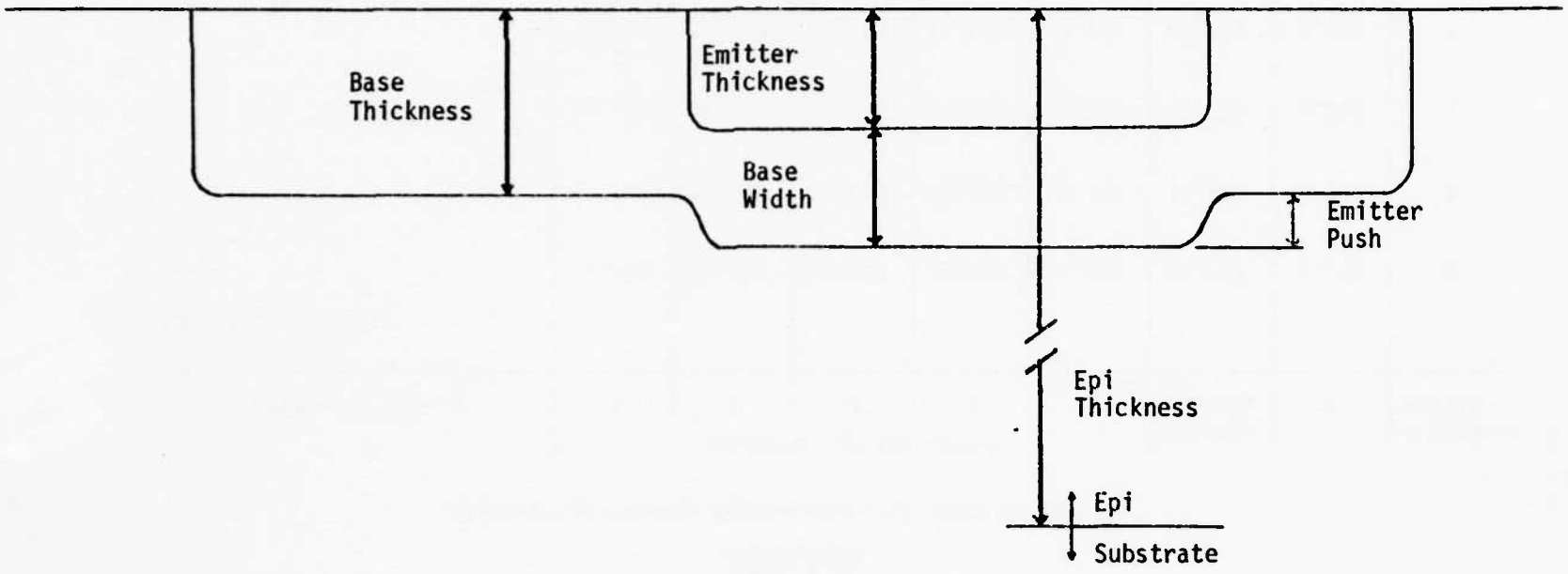
Base
Thickness
Emitter
Thickness
Base
Width
Emitter
Push
Epi
Thickness
Epi
Substrate

FIGURE 4.22a

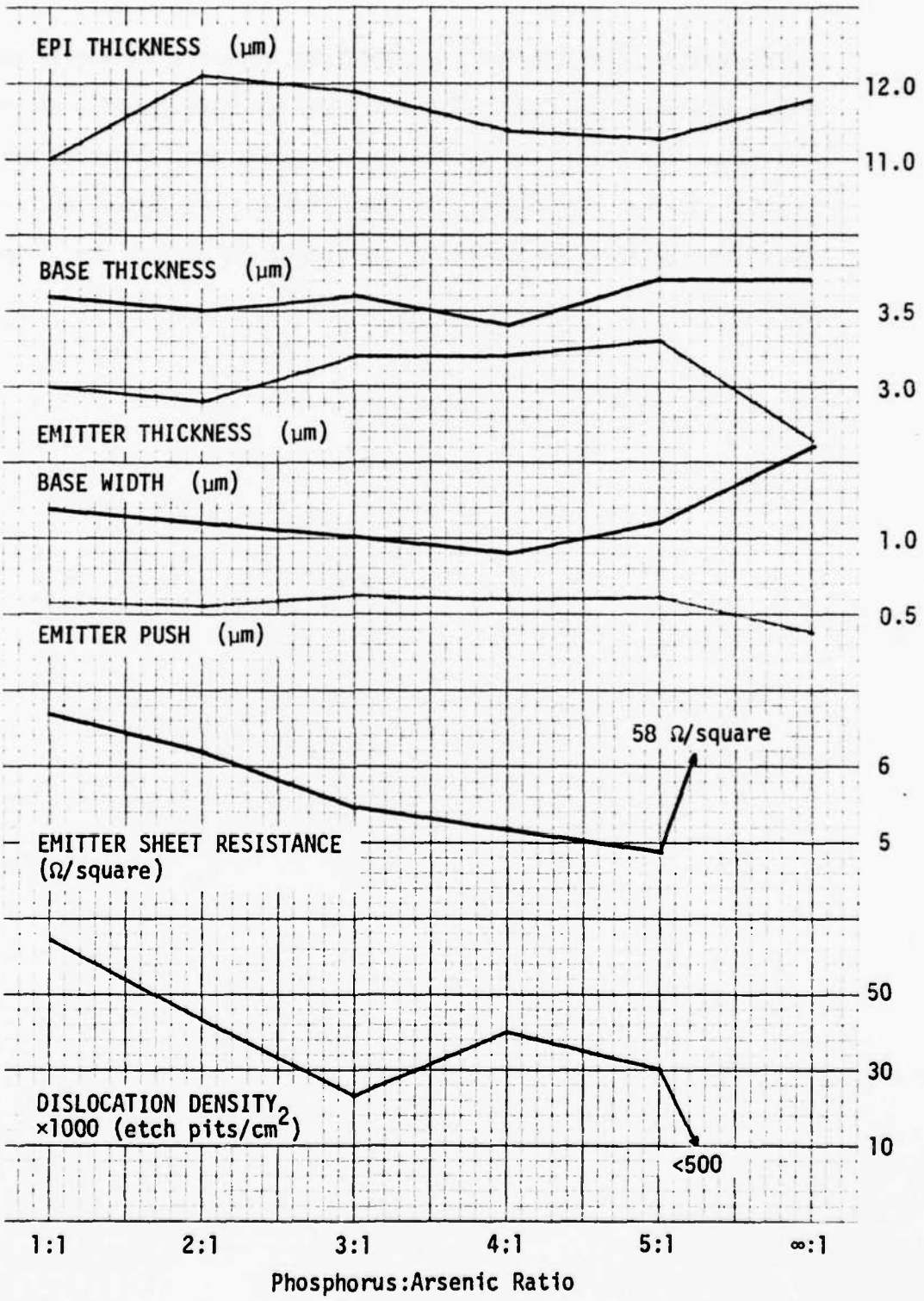

FIGURE 4.22b

Summary of the Second Dual Dopant Transistor Measurements

the dislocation densities of the unprocessed wafers), indicating that the Wright etch mixed and used in our study may not have revealed all the dislocations. Striation-like surface texturing was again observed after dislocation etching. The dislocation densities did not significantly decrease toward the center of the wafers in the second set of dual dopant transistors.

CHAPTER 5

DISCUSSION

The present study differed from the M. Watanabe et.al. [3] work in two major aspects. Our study investigated the effects of simultaneous phosphorus and arsenic drive-in diffusions from predeposition diffusions using dual dopant SiO_2 spin-on sources on emitter push and dislocation generation. The M. Watanabe et.al. study investigated the effects of simultaneous phosphorus and arsenic predeposition diffusions (i.e., without drive-in diffusions) using CVD dual dopant SiO_2 sources on emitter push and dislocation generation. The results of our study suggests that the differences in the dopant sources and diffusion conditions between our study and the M. Watanabe et.al. study may have had profound effects on emitter push and dislocation generation. It is recognized that simultaneous diffusion technology is presently in the early stages of development and there may well be other phenomena in addition to those suggested by our study and the M. Watanabe et.al. study involved in simultaneous diffusions that affect emitter push and dislocation generation.

The behavior of the interface between the dopant source and silicon surface is not well understood. A reduction in emitter push was reported [24] when the phosphorus predeposition diffusion was performed through a thin polycrystalline silicon film. It was postulated that the polycrystalline grain boundaries at the polycrystalline to crystalline silicon interface adsorbed the excess point defects created by the phosphorus diffusion and thus emitter push was reduced. One could also speculate that the CVD dual dopant SiO_2 source to silicon interface has similar adsorbing properties while the dual dopant SiO_2 spin-on source to silicon interface

does not. The cloudy surface of spin-on diffused layers indicate that the spin-on sources used in our study may be changing the silicon surface, thus affecting interface properties.

The pile-up of arsenic atoms at off-lattice sites observed by M. Watanabe et.al. was reported to occur at high phosphorus/arsenic concentrations. Our drive-in diffusions (the M. Watanabe et.al. investigation did not incorporate drive-in diffusions) may have sufficiently lowered the surface dopant concentration to move the pile-up, off-lattice site arsenic atoms to substitutional positions (i.e., annealing the lattice damage). Since the pile-up of arsenic atoms at off-lattice sites are believed to provide strain compensation at the surface of the simultaneous phosphorus and arsenic predeposition diffused layer, such an annealing effect during a drive-in diffusion may generate point defects that cause emitter push to occur.

Our proposed drive-in diffusion annealing effect may also affect the simultaneous diffusion dislocation generation prevention mechanism at the surface of the dual dopant diffused layer as proposed by M. Watanabe et.al. and evidenced by our observed high dislocation densities. Nonetheless, our measured dislocation densities were minimized near the optimum dual dopant source ratios reported by M. Watanabe et.al., indicating that dislocation generation may have been reduced during our dual dopant spin-on source predeposition diffusions. One could speculate that dual dopant drive-in diffusions may have enhanced dislocation generation properties that created our observed high dislocation densities.

The epitaxial material used in our study may not have minimized the fluctuation in wafer material sheet resistance which was believed to be one of the causes of variation in transistor gain. Our attempts to monitor the

epitaxial layer sheet resistance uniformity using four point probe techniques failed (possibly due to the thinnest and high resistivity of the epitaxial layer). The extensive surface texturing of the Epitaxy wafer surface after the dislocation etching and the lower gain of Epitaxy transistors compared to simultaneously fabricated Wacker wafer transistors indicated that the Epitaxy material may have been of poorer quality than the Wacker material. The variation in transistor gain may have also been due to many other factors including nonuniform doping from the spin-on sources, temperature and other ambient variations during processing, and systematic processing errors.

CHAPTER 6

CONCLUSIONS AND RECOMMENDATIONS

The preliminary results from our study indicates that the simultaneous diffusion of phosphorus and arsenic from dual dopant SiO_2 spin-on sources to improve device performance may be applicable to commercial diffusion techniques which commonly involves predeposition and drive-in diffusions. Both our study and the M. Watanabe et.al. study are early attempts to investigate this new processing technology and although neither study can be considered comprehensive, both studies suggest promise for the new technology. Our study monitored the simultaneous phosphorus and arsenic diffusions after drive-in diffusions from predeposition diffusions using dual dopant SiO_2 spin-on sources. Although we observed no consistent evidence that the simultaneous diffusions reduced emitter push and the dislocation density of the dual dopant diffused layer surface was very high, a reduction in dislocation density in dual dopant diffused layer surfaces was observed near the 3:1 dual dopant source ratio. Additional studies are recommended to clarify the inconsistent emitter push results of our study.

The results of our study were derived from a materials science approach to monitor the effects of the simultaneous diffusions. The problems with the transistor gain measurements denied our study valuable information about the electrical effects of the simultaneous diffusions. Subsequent investigations of simultaneous diffusions would be enhanced using electrical monitoring techniques to directly observe possible improvements in device performance.

The difference in the results between our study and the study of M. Watanabe et.al. indicates that the phosphorus to arsenic ratio in the

SiO_2 source is not the only parameter affecting emitter push and dislocation generation. Diffusion conditions, interface properties between the dopant source and silicon, and other phenomena not apparent at this time may also affect emitter push and dislocation generation. Additional investigations should also monitor the effects of the simultaneous diffusions after a predeposition diffusion using the dual dopant SiO_2 spin-on sources. Such measurements may help disclose if diffusion conditions and dopant source to silicon interface properties affect emitter push and dislocation generation.

APPENDIX A

SHEET RESISTANCE MEASUREMENTS

Sheet resistance was measured using the conventional four point probe technique. Sheet resistance measurements were taken at five positions on each wafer quarter to monitor the sheet resistance uniformity. Figure A.1 shows the approximate locations of the four point probe measurements. The measurements near the wafer periphery were at least five probe spacings from the wafer edge to minimize measurement error. At each position the current increments used to measure the sheet resistance were 0.25, 0.50, 2.5, 5.0, and 10.0 milliamperes and the resultant voltages recorded. The following relation was used to determine the sheet resistance, ρ_s' :

$$\rho_s' = \frac{\pi}{\ln 2} \frac{V}{I}$$

from the current and measured voltages. The polarity of the current was reversed at each measurement to eliminate rectifying point contact effects.

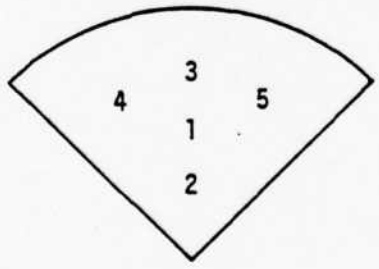

FIGURE A.1

Position of the Four Point Probe Measurements

The five sheet resistance measurements at each position were averaged and represented positional sheet resistances. These five positional sheet resistances were averaged, $\overline{\rho_s}'$, and standard deviation determined. The following formula was used to determine the standard deviation, $\overline{x}$:

$$\overline{x} = \left[\frac{\sum_{i=1}^{n} x_i^2 - \frac{1}{n} \left[\sum_{i=1}^{n} x_i \right]^2}{n - 1} \right]$$

The average sheet resistance represented the wafer or diffused layer sheet resistance and the standard deviation was used to monitor the sheet resistance uniformity.

APPENDIX B

WAFER CLEANING PROCEDURE

Process	Time
10:1 diluted HF dip to remove thermal oxide	10 - 15 seconds
D.I. (Deionized wafer) bath with periodic agitation to rinse off the HF	10 minutes
Acationox/D.I. bath using ultrasonic agitation and camel hair brush to swab the surface to remove organic contamination	1 minute
Thorough D.I. rinse to remove the surfactant	
H_2SO_4/H_2O_2 bath to remove ionic contaminations, solution should be hot	2 minutes
D.I. bath with periodic agitation to rinse off the H_2SO_4/H_2O_2	10 minutes
Second D.I. bath with periodic agitation to rinse off the H_2SO_4/H_2O_2	10 minutes
Spin dry the wafer Start at low speed and slowly accelerate to remove the D.I. and to minimize splash back	

APPENDIX C

TRANSISTOR FABRICATION SCHEDULE

Description	Process
Clean wafer	see Appendix B
Base definition oxide	wet oxide, 1 hour at 1100°C oxide thickness ~ 5000 Å need ~ 2000 Å to block the boron base predeposition diffusion
Base window definition	positive photoresist, see Appendix C3, using the mask on Figure 4.4d and etch windows
Clean wafer	
Base predeposition diffusion	see Appendix C1, 1/2 hour at 950°C ambient: N_2
Remove doped glass	10:1 diluted HF dip, 15-30 seconds and D.I. bath for 10 minutes
Base drive-in diffusion and emitter definition oxide	2 hours at 1150°C ambient: O_2 for initial 80 minutes N_2 balance oxide thickness ~ 2000 Å need ~ 1000 Å to block the phosphorus emitter predeposition diffusion
Emitter window definition	negative photoresist, see Appendix C3 using the mask on Figure 4.4e and etch windows

Description	Process
Clean wafer	
Emitter predeposition diffusion	see Appendix C2, 1/2 hour at 950°C ambient: 95% N_2, 5% O_2
Remove doped glass	10:1 diluted HF dip 15-30 seconds and D.I. bath for 10 minutes
Emitter drive-in diffusion and contact windows definition oxide	2 hours at 1100°C ambient: O_2 for initial 45 minutes N_2 balance oxide thickness ~ 1000 Å
Contact windows definition	negative photoresist using the mask on Figure 4.4f and etch windows
Clean wafer	
Metallize	vacuum evaporation of aluminum
Metallization definition	positive photoresist using the mask on Figure 4.4g and etch away unwanted metal
Sinter contacts	3 minutes at 450°C ambient: N_2

All high temperature processes utilized a slow push/pull to minimize thermal stresses in the wafer. The 3-4 inch per minute push/pull rate took approximately 7 minutes. This push/pull time was added to the processing time.

APPENDIX C1

BORON PREDEPOSITION

The planar deposition source used was manufactured by the Carborandum Company. The combat boron nitride, grade BN-975, source used is recommended for the 950°C predeposition temperature. The recommended boron nitride wafer cleaning procedure used is as follows:

Process	Time (minutes)
Trichloroethylene degrease	5
Acetone solvent rinse	2
D.I. rinse	5 (maximum)
Concentrated HF clean	1
D.I. rinse	5 (maximum)
Dry, 350°C - 400°C , dry N_2 ambient	1 hour

The drying time was increased to 24 hours to thoroughly dry out the wafers. Prior to each predeposition the boron nitride wafers were oxidized (1/2 hour at predeposition temperature in dry O_2) to produce B_2O_3 glass and stabalized (1/2 hour minimum at predeposition temperature in dry O_2) to homogenize the B_2O_3 glass layer. After stabalization the boron nitride wafers were ready to be used for predeposition.

APPENDIX C2

EMITTER PREDEPOSITION

The wafers were cleaned using the wafer cleaning procedure outlined in Appendix B prior to applying the spin-on dopant solution. The surface should be hydrophilic for Emulsitone sources and water repellent for Accuspin (Allied Chemical) sources. The Emulsitone sources required no additional treatment after wafer cleaning since the H_2SO_4/H_2O_2 bath leaves the surface hydrophilic. A 10:1 diluted HF dip followed by a ten minute D.I. rinse is needed for the Accuspin sources to render the surface water repellent.

The wafer is placed on the spinner chuck and several drops of spin-on dopant solution are applied and allowed to spread and cover the top of the wafer. The wafer is then spun at 3000 rpm for 15 seconds using a 200 millisecond acceleration interval. The spin-on applications were performed in the fume hood.

The coated wafers were then placed at the mouth of the preheated (950°C predeposition temperature) oxide furnace tube and left there for 15 minutes to cure the spin-on film (bake out solvents). After the film was cured, the wafers were pushed to the center of the tube for the predeposition diffusion. The 95% N_2 and 5% O_2 ambient was recommended by both manufacturers and used during both film curing and predeposition diffusion.

The spin-on dopant solutions were stored in all polypropylene dropping bottles. Between uses the spin-on solutions were stored in a freezer to prolong their shelflife.

APPENDIX C3

PHOTORESIST PROCEDURE

KTl Negative Photoresist Procedure

Process	Method	Time	Temperature
Coat wafer	Spin at 4000 RPM	15 seconds	Room temperature
Air dry	Under laminar flow hood	3 minutes	
Prebake the resist coating		25 ± 5 minutes	90 ± 5°C
Expose		5-7 seconds	
Develop	Soak in KTl developer	1 minute	
Rinse	Immerse in KTl rinse	30 seconds	
Dry	N_2 blow dry		
Postbake the resist coating		25 ± 5 minutes	140 ± 5°C
Etch	Buffered HF (oxide)		
Strip off the resist coating	Immerse in H_2SO_4/H_2O_2 solution	30 seconds	

Shipley AZ-13605 Positive Photoresist Procedure

Process	Method	Time	Temperature
Coat wafer	Spin at 4000 RPM	15 seconds	Room temperature
Air dry	Under laminar flow hood	3 minutes	
Prebake the resist coating		15 minutes	90°C
Expose		5-7 seconds	
Develop	Soak in Shipley AZ-606 developer	25 seconds	
Rinse	Immerse in deionized water	25 seconds	
Dry	N_2 blow dry		
Postbake the resist coating		15 minutes	90°C
Etch	Buffered HF (oxide) Al etch (aluminum)		
Strip off the resist coating	Immerse in Shipley 1112-A remover	30 seconds	

Composition of the Oxide and Al Etches

Buffered HF: (Oxide etch)	Ammonium Fluoride	(NH_4F)	450 grams
	Hydrofluoric Acid	(HF)	100 milliliters
	Deionized Water	(H_2O)	660 milliliters
Aluminum etch:	Phosphoric Acid	(H_3PO_4)	20 parts
	Nitric Acid	(HNO_3)	1 part

APPENDIX D

QUARTZ, GLASS, AND PLASTIC LABWARE CLEANING PROCEDURE

All quartzware associated with the diffusion furnace including diffusion and oxide tubes, tube end caps, boats, boat holders, push rods, and bubblers were cleaned by etching in a 10:1 diluted HF bath for half hour followed by half hour D.I. bath and final liberal rinsing with D.I. Glassware associated with the diffusion furnace including push rod holders and bubblers were clean in a similar fashion, except the half hour 10:1 diluted HF bath was reduced to 15 minutes.

Plastic and other glass labware were cleaned using a H_2SO_4/H_2O_2 bath followed by a water rinse and final D.I. rinse. This method was used each time the quartzware was etched. Between etchings, the glass and plastic labware were cleaned by scrubbing with a beaker brush and Acationox. The surfactant was rinsed off with tap water then finally with D.I.

APPENDIX E

LAP AND STAIN PROCEDURE

The lapping jig used was a standard bevel-polishing fixture with a bevel angle of 2.3^{0}. Several lapping compounds and slurries were tested to determine which produced a good polished surface with minimum effort. A water based slurry was chosen composed of:

Linde A (0.3 μm alumina abrasive)	1 gram
Joy (detergent)	2 milliliters
Water	15 milliliters

A quarter inch thick glass plate was used as the polishing plate. The plate was roughly polished with 600 grit silicon carbide using the outer ring of the bevel-polishing fixture and subsequently finer polishes were used to obtain a flatter polishing plate. Specimen samples used to chip and fracture during lapping before the plate was ground flatter.

The lapping procedure is as follows:

1. Dice up the wafer into manageable sizes (two transistors per die).
2. Heat the lapping jig insert with a propane torch and apply a thin layer of Apiezon black wax.
3. Place the specimen on the heated wax and use a tweezer to position the specimen using a circular motion to expel excess wax from under the specimen. Place the insert into the outer ring of the bevel-polishing fixture, cool end first to facilitate cooling.
4. Wet the polishing plate and apply a few drops of the lapping slurry. The insert is placed on the polishing plate with the specimen away from the plate and the entire fixture is slowly set upright.

5. Applying moderate pressure to the insert with one finger and move the fixture in a figure eight or circular motion. The amount of material removed is checked by periodic inspection of the specimen under an inspection microscope.

6. The specimen is removed by heating the insert with the propane torch and sliding the specimen off. The specimen should be thoroughly rinsed with deionized water prior to removal to minimize residue on the lapped surface.

The staining procedure is as follows:

1. The tapped specimen should be stained as soon as possible after lapping to obtain best results.

2. The following procedure was used to clean the lapped specimen:

Process	Time
Trichloroethane bath to remove the black wax	5 minutes
Trichloroethane rinse	
Methanol bath, solvent rinse	1 minute
Deionized water bath	10 minutes
H_2SO_4/H_2O_2 bath	3 minutes
Deionized water bath	10 minutes
Deionized water bath	10 minutes

3. Blow dry the specimen with dry N_2. Other types of stains may work better with wet specimens.

4. Immerse the specimen in a small quantity of 50-6 Cu stain. Illuminate the specimen with intense light to minimize junction width and sometimes enhance staining. Optimum staining occurred in approximately fifteen seconds.

The composition of the 50-6 Cu stain is:

50-6 stain	10 milliliters
2 drops	Cu*

50-6 stain:	Hydrofluoric Acid (HF)	50 milliliters
	Nitric Acid (HNO_3)	6 drops
Cu^* :	Copper Nitrate ($Cu(NO_3)_2$)	20 gram
	Water (H_2O)	80 milliliters
	Hydrofluoric Acid (HF)	1 milliliter

5. The stain is diluted with a large quantity of deionized water to stop the staining. The specimen is rinsed off with deionized water, placed in a ten minute deionized bath, and then blown dry with N_2 gas.

The junction depths were measured using a microscope with a 15X eyepiece, 1.5X epi-illuminator stage, and 5X, 10X, and 20X objective lenses. Two ocular pieces, a 10 mm grid pattern (0.5 mm/grid) and a 10 mm linear scale (0.05 mm/division), were mounted together to facilitate measurements. The ocular stages were calibrated with a 2 mm linear stage micrometer (0.01 mm/division). The following calibrations were obtained:

Objective Power	μm/grid
5X	66.0
10X	33.0
20X	16.5

The junction depth was calculated using the following formula derived from geometric considerations:

$$x_j = (\text{number of grids})\ (\mu\text{m/grid})\ \tan\ 2.3^{o}$$

The measurement error is ± 0.05 mm on the linear scale ocular piece or 0.1 grid which corresponds to:

Objective Power	Δ xj (μm)
5X	0.27
10X	0.13
20X	0.07

A 0.1^{o} change in angle of the bevel corresponds to a 5% change in the actual junction depth.

There are other methods that have much higher resolution. However, the outlined measuring technique was sufficient to meet the needs of our study.

APPENDIX F

DISLOCATION ETCH AND DENSITY DETERMINATION PROCEDURE

The Wright etch was used to delineate dislocations. The Wright etch worked well on both (111) and (100) wafers, producing triangular dislocation etch pits in (111) wafers and elliptical pits in (100) wafers. There was also very little extraneous surface texturing. The composition of the Wright etch is:

Hydrofluoric Acid	(HF)	60 milliliters
Nitric Acid	(HNO_3)	30 milliliters
5 Molal Chromic Trioxide	(CrO_3)	30 milliliters
(15 gms. CrO_3 and deionized water to produce 30 ml. of solution)		
Copper Nitrate	($Cu(NO_3)_2$	2 grams
Acetic Acid	(CH_3 (OOH)	60 milliliters
Water	(H_2O)	60 milliliters

No specifc order to mix the etchant is necessary and the Wright etch has a shelf life of four weeks.

Each wafer section was etched in approximately 15 ml. of etchant. The etchant was hand agitated to prevent the redeposition of etched silicon onto the wafer surface. The etchant removed approximately 1 μm of silicon material per minute. The fifteen minute etch produced easily seen pits (approximately 10 μm long pits (100) wafers).

The dislocation density was determined by counting all the etch pits visible in the microscope field of view and dividing the field count by

the area of the microscope field. The dislocation density was measured at five positions on the wafer quarters to monitor the uniformity of dislocation formation. Figure F.1 shows the approximate locations of the dislocation density measurements.

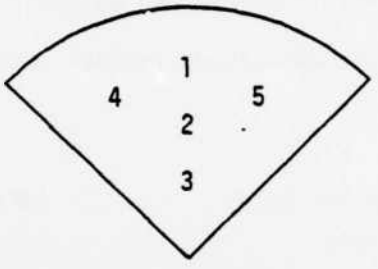

FIGURE F.1

Position of the Dislocation Density Measurements

APPENDIX G

DUAL DOPANT SPIN-ON MIXING PROCEDURE

The phosphorosilicafilm (PSF) used to formulate the dual dopant sources was a stock item manufactured by Emulsitone Company and reportedly produced a $C_s = 1 \times 10^{21}$ electrically active phosphorus atoms per cm^3. The PSF spun-on film and solution reportedly had 1.6×10^{22} phosphorus atoms per gram SiO_2. The arsenosilicafilm (ASF) used in the dual dopant sources was a special mix formulated such that the arsenic atom concentration per gram SiO_2 and the concentration of SiO_2 in the ASF solution were the same as the PSF. The specifications of the PSF and ASF sources are listed in Table G.1. The formulation of the ASF was so chosen to facilitate mixing the dual dopant sources.

A 1:1 ratio of phosphorus to arsenic in the dual dopant source was obtained by mixing one part of PSF to one part of ASF producing 8.2×10^{21} of each dopant species per gram SiO_2. This concentration of phosphorus atoms per gram SiO_2 was maintained while the arsenic concentration was varied to change the phosphorus to arsenic ratio in the dual dopant source. For example, a 3:1 ratio was obtained by mixing three parts of PSF, one part of ASF, and an appropriate amount of silicafilm (SF) to maintain 8.2×10^{21} phosphorus atoms per gram SiO_2 in the dual dopant source. Five milliliter solutions of each of the dual dopant sources were mixed using two milliliter pipets with 0.01 milliliter accuracy. The mix ratios and amounts used to formulate the dual dopant sources are tabulated in Table G.2.

Calculations were performed using the published weight percentages and solution densities to determine the phosphorus to arsenic dual dopant source

ratios and dopant atoms per gram SiO_2 listed in Table G.2. The calculated phosphorus atoms per gram SiO_2 was close to the published specifications (Table G.3). The calculated arsenic concentration was 20% higher than the published specifications changing the resultant calculated phosphorus to arsenic dual dopant source ratio. It was assumed that the published dopant atom concentrations per gram SiO_2 were correct and the mix amounts in Table G.2 used.

The dual dopant solutions were stored in 30 milliliter all polypropylene dropping bottles. The dropping bottles were stored in ziplock bags to prevent absorbtion of moisture by the spin-on solution. The spin-on solutions were stored in a freezer to increase shelf life. The spin-on solutions were allowed to come to room temperature prior to application.

TABLE G.1

Spin-On Dopant Specifications

Phosphorosilicafilm, $C_s = 1 \times 10^{21}$
Lot Number 09180

Spin-on Solution: 8.74 wt. % P_2O_5
4.54 wt. % SiO_2
Density = 0.88 gm/cc

Glass Film: 1.6×10^{22} phosphorus atoms per gm SiO_2

Arsenosilicafilm, Special Mix
Lot Number 09220

Spin-on Solution: 14.2 wt. % As_2O_3
4.54 wt. % SiO_2
Density = 0.88 gm/cc

Glass Film: 1.6×10^{22} arsenic atoms per gm SiO_2

Silicafilm
Lot Number 10309

Spin-on Solution: 7.0 wt. % SiO_2
Density = 0.88 gm/cc

TABLE G.2

Mix Ratios for the Dual Dopant Sources

Dual Dopant Source	Composition	Amounts Mixed for 5 ml solutions (ml)
PSF, dilute	1 part PSF	3.03
	0.65 part SF	1.97
ASF, dilute	1 part ASF	3.03
	0.65 part SF	1.97
1:1, P:As	1 part PSF	2.50
	1 part ASF	2.50
2:1, P:As	2 parts PSF	2.74
	1 part ASF	1.38
	0.65 part SF	0.89
3:1, P:As	3 parts PSF	2.83
	1 part ASF	0.94
	2(0.65) part SF	1.23
4:1, P:As	4 parts PSF	2.88
	1 part ASF	0.72
	3(0.65) part SF	1.40
5:1, P:As	5 parts PSF	2.91
	1 part ASF	0.58
	4(0.65) part SF	1.51

TABLE G.3a

Calculated Dopant Atoms Per Gram SiO_2

Spin-On Source	Published Dopant Atoms/gm SiO_2	Calculated Dopant Atoms/gm SiO_2
PSF, $C_s = 1 \times 10^{21}$	1.6×10^{22}	1.6×10^{22}
ASF, Special Mix	1.6×10^{22}	1.9×10^{22}

TABLE G.3b

Calculated P:As Dual Dopant Ratios

Dual Dopant Source	Calculated P:As Ratio
1:1, P:As	0.9:1
2:1, P:As	1.8:1
3:1, P:As	2.7:1
4:1, P:As	3.5:1
5:1, P:As	4.5:1

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